Shanghai Fudan Microelectronics Group Company Limited

复旦微电子

FM33A0xxEH

Smart Metering MCU

Brief Datasheet

2024. 3

Contents

1 Product Overview

1.1 Outline

This document is a brief datasheet for FM33A0xxEH, which is a 32bit Cortex-M0+ with max 512KB+512KB eFlash and 96KB SRAM. FM33A0xxEH also integrates 12bit 2Msps SAR-ADC, Comparators, CAN2.0B, UART w/ LIN support.。

Features：

- Operating Voltage Range: 1.8~5.5V
- Operating Temperature Range (T_A): -40℃~+105℃
- Processor
  - ARM Cortex-M0+ up to 80MHz
  - User/Priviledged mode
  - Support MPU
  - NVIC
  - SWD debug interface
  - 24bit Systick
- Typical current consumption
  - Active：100uA/MHz typical
  - Sleep：50uA typical
  - DeepSleep：3.5uA typical
- Memory
  - Max 1024KB code flash
  - Flash endurance: 100,000cycles
  - Code protection mechanism
  - Up to 96K bytes RAM
- Rich Analog
  - Highly Reliable Programmable BOR
  - Ultra-low-power PDR
  - Programmable Supply Voltage Detector
  - 2xComparator
  - 14bit 2Msps SAR-ADC up to 14 external inputs
  - Temperature Sensor linearity +/-2℃
- Communication interfaces
  - UART*10, 4 support LIN
  - LPUART*2

- SPI*5, master/slave
- I2C*2, master/slave
- I2C_SMBUS*2
- CAN2.0B*3, CAN-FD*1
- 11-channel peripheral DMA
- Prgrammable CRC
- Timers
- 16bit Advance Timer*2
- 16bit Timer Array
- 32bit Basic timer*1
- 24-bit Systick*1
- 16bit Low-power timer*1
- Windowed watchdog timer*1
- Independent watchdog timer*1
- Real-time clock calendar (RTCC), w/ clock calibration +/-0.06ppm

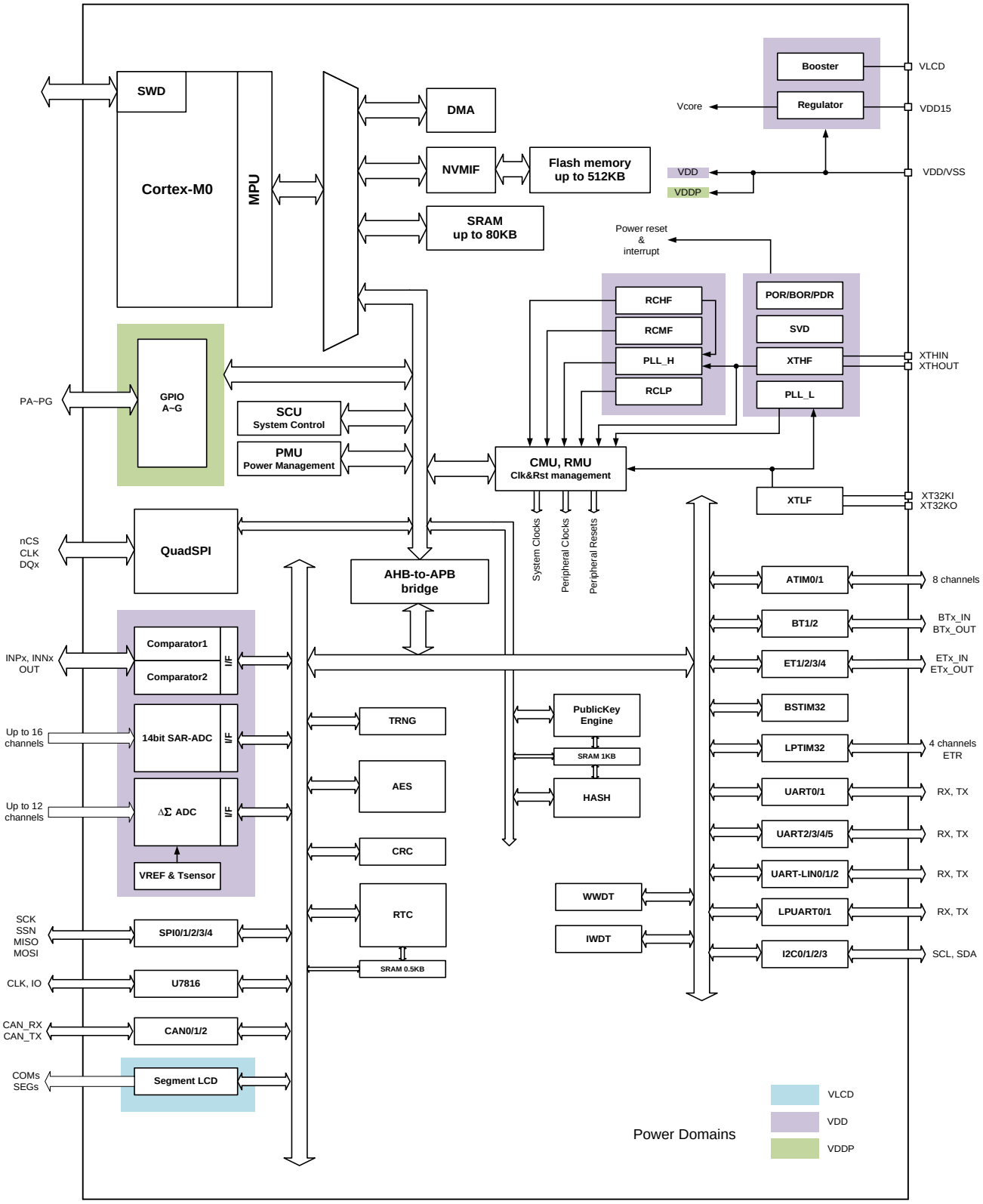
- LCD Driver
  - Up to 4COM×44SEG / 6COM×42SEG / 8COM×40SEG
  - 1/3 Bias, 1/4 Bias
  - Internal buffer mode or external capacitor mode
  - Internal VLCD voltage booster
  - Display under SLEEP
- Security features
  - Hardware AES accelerator, 128/192/256-bit
  - Supporting ECB/CBC/CTR/GCM/GMAC mode
  - Public key cryptography algorithm acceleration engine: Support ECC192/256/384/512, RSA2048
  - HASH : supports SHA-1, SHA-256
  - True Random Number Generator
- Clock generation
  - High-speed RC oscillator, 8/16/24/32MHz factory trimmed to +/-0.5%，8/16MHz full-temperature variation is less than +/-2%
  - Low power 32.768Khz crystal oscillator with fail detector
  - Low-speed RC oscillator, 32Khz
  - High speed crystal oscillator 8~24MHz
  - PLL_H, max 80MHz
  - PLL_L，16.384MHz

1.2 Device Lineup

Part code	Flash（KBytes）	RAM（KBytes）	Package
FM33A0XXEH	1024	96	LQFP100

Table 1-1FM33A0XXEHdevice lineup

1.3 Block Diagram



FM33A0XXEH structure diagram

1.3.1 Pinouts and pin description

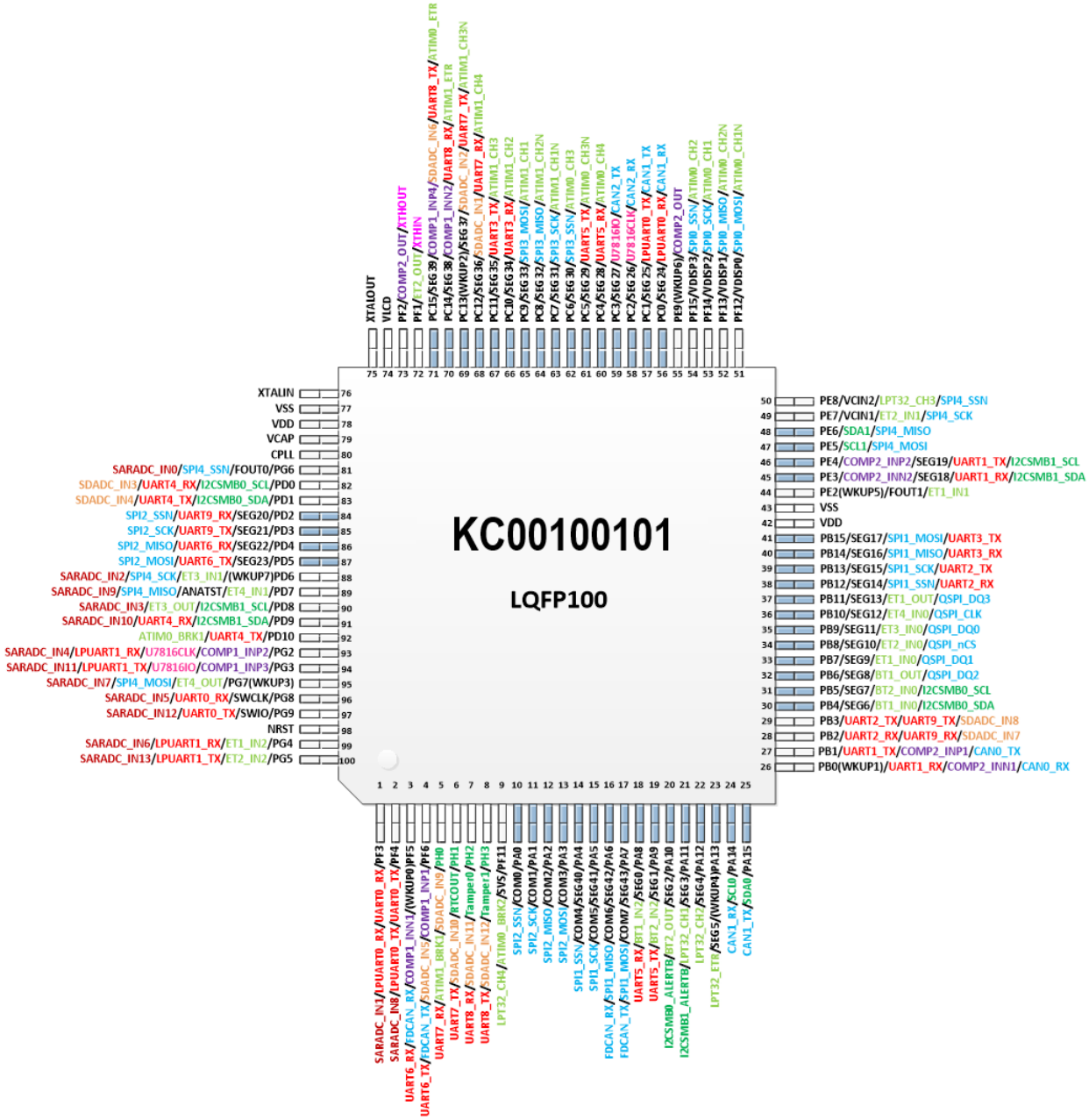


Figure 2-1 FM33A0XXEH LQFP100 pinout

NOTE:

Blue pins are 5V-tolerant(FT), which can stand voltage higher than VDD without leakage current.

1.3.2 Package size drawing

1.3.2.1 LQFP100

MPQ：900PCS

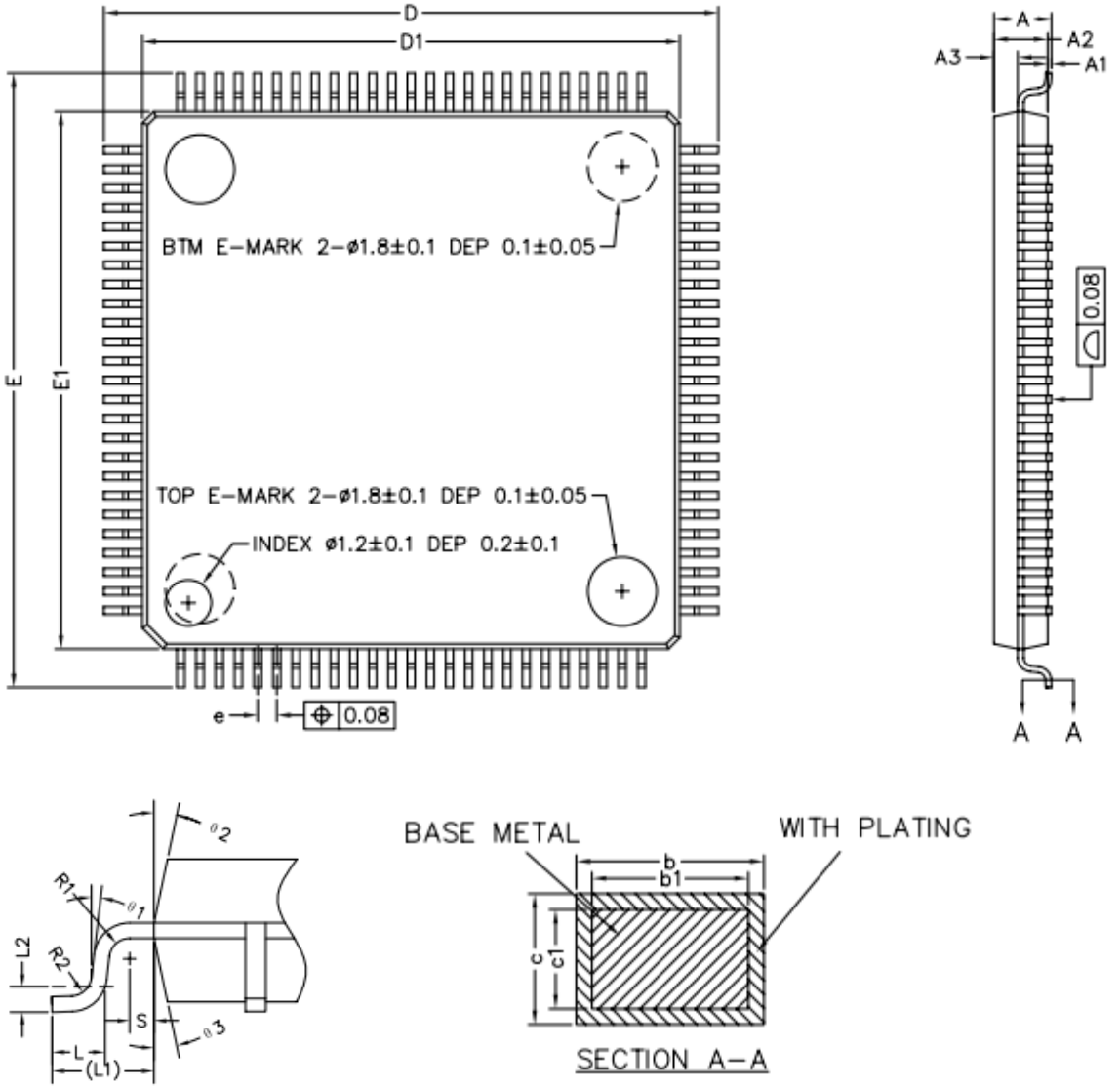
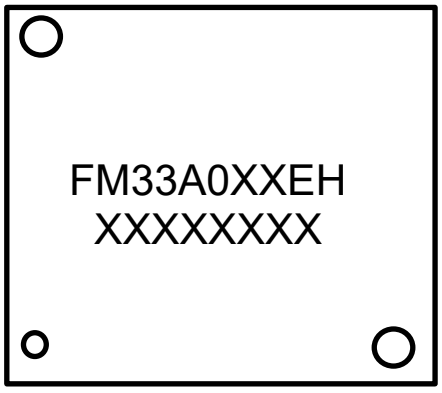


图 Figure 1-2 LQFP100 Package size drawing

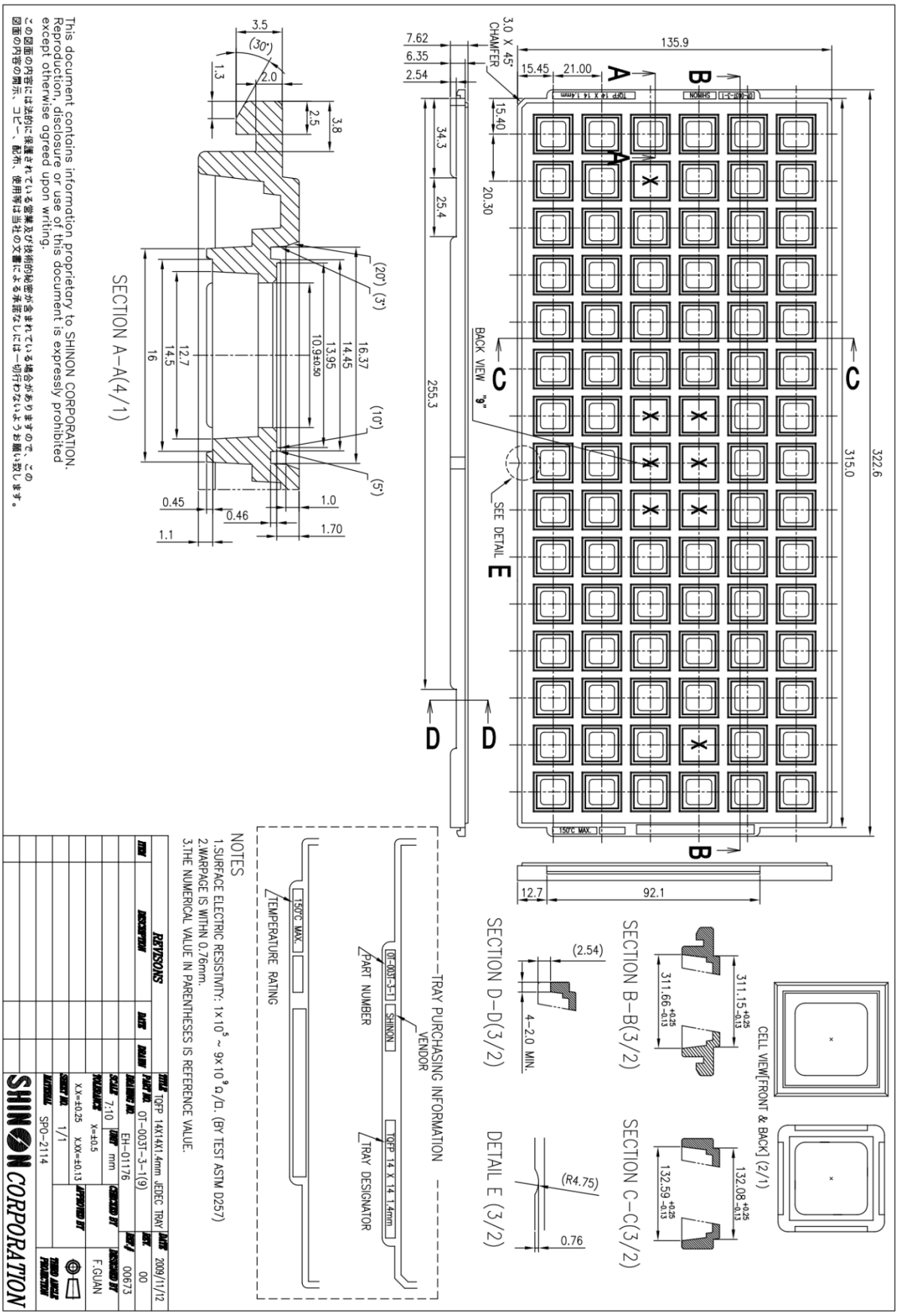
Symbol	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTE:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BDD.

1.3.2.2 Marking instructions



FM33A0XXEH:MPN
xxxxxxxx:Wafer batch information



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2 Flash memory protection

Flash memory protection can be used to protect user code, user data and user configuration information in Flash from being read or tampered with by unauthorized third party. Flash Protection includes two types: DBRDP-Debug ReaD Protection and ACLOCK-Application Code Block Locking.
Flash protection is controlled via OPTBYTES in LDT1.

2.1 Debug interface protection（DBRDP – DeBug ReaD Protection）

The primary purpose of DBRDP is to prevent unauthorized access to the Flash content through the Debug interface.
DBRDP is enabled or disabled by the OPTBYTES.DBRDPEN configuration word in LDT1 page (0xAA means DBRDP is disabled, which is default state of a fresh device).
There are two levels of DBRDP: basic protection and fuse protection

Disable DBRDP： no protection
Flash can be read, erased, and programmed through the SWD interface.

Basic protection level:
Flash main array cannot be read or erased or programmed via the SWD interface.
How to exit basic protection: Perform full-space matrix erase through SWD. After matrix erase is completed, SWD can modify OPTBYTES to disable DBRDP, and then reset the chip.
After reset the chip will be in no protection state.

Fuse protection:
Under fuse protection, the SWD is permanently disabled.This means FudanMicro is unable to perform any failure analysis on the chip. In the case of fuse protection, the Debugger cannot establish a connection with the CPU anymore.

2.2 ACLOCK – Application Code Lock

The main purpose of ACLOCK is to prevent any unauthorized reading or tampering to the application code in Flash from hacking code. With the ACLOCK function, you can set some part of flash as fetch-ony, any read-as-data or modifying are prohibited. ACLOCK works in the granularity of 8KB. The whole Flash contains 32 Blocks with 2bit LOCK information for each Block. The default LOCK word is 0xFFFF_FFFF for a fresh device, which is unprotected. When the corresponding LOCK bits are set to 01 or 10, this block can only be fetched by CPU. When the corresponding LOCK bits are 00, both CPU and SWD are prohibited to read or modify the block. ACLOCK function is disabled by default. The user needs to enable ACLOCK through the programmer, and the user code should conform to the ACLOCK configuration when compiling (for example, literal pool cannot be compiled to the locked Block).

Functions of ACLOCK：

- No protection： All blocks allow CPU to fetch, read, and modify. No restriction on SWD access.
- Read-write protection: specified blocks allow CPU to fetch only, read & modify by CPU and DMA is prohibited. No restriction on SWD access.

- Software and SWD protection: specified blocks allow CPU to fetch only, read & modify by CPU, DMA and SWD is prohibited.

The relationship between LOCK bit and Block access permissions is shown in the following table:

LOCK bit	CPU read	CPU fetch	SWD read and erase/program
11	√	√	√
01/10	×	√	√
00	×	√	

ACLOCK information is loaded into registers after system reset. These registers can also be set by software, but cannot be cleared by software (it is only possible for software to escalate the protection level).
LOCK register contents are invalid when ACLOCK is not enabled.

Note: *ACLOCK is independent of DBRDP for each Block in Flash. For SWD interfaces, DBRDP has higher priority than ACLOCK, that is, after DBRDP is enabled, SWD cannot access Flash regardless of whether ACLOCK is enabled or not.*

Exit ACLOCK: Full-space matrix erase must be performed by SWD. After matrix erasing, SWD can modify OPTBYTES to disable ACLOCK, and then reset the chip. After reset, ACLOCK is unactivated

3 Debug Support

3.1 Introduction

The chip is based on the ARM Cortex-M0 processor and supports the corresponding debug features. Through hardware breakpoints (breakpoints) and data watchpoints (watchpoints), the debugger can stop the CPU core operation during specific instruction fetches and data accesses, inspect the core registers and system peripheral state, and resume the core operation as needed.

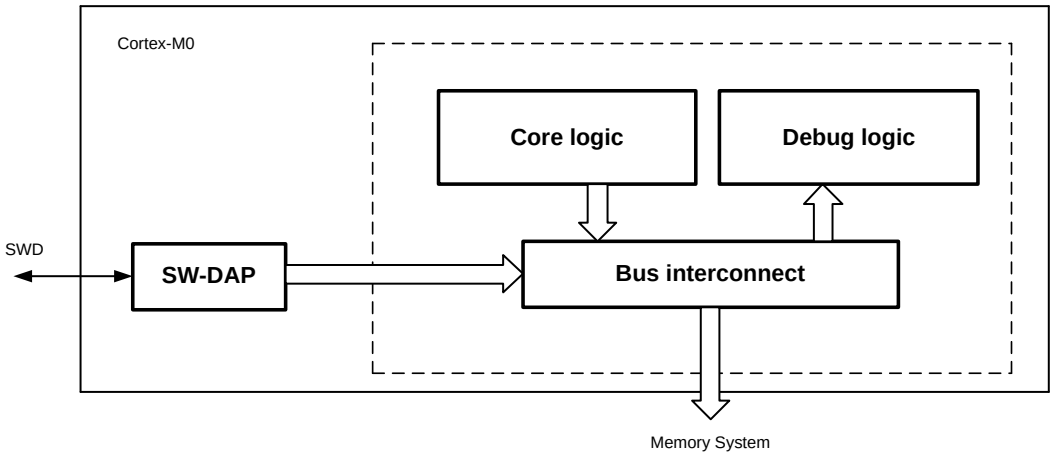


Figure 3-1 Cortex-M0 debug system diagram

For debug features of the Cortex-M0 core, please refer to the Cortex-M0 Technical Reference Manual from ARM.

3.2 Debug Pin

3.2.1 SWD Pin

The SWD pins of this chip are as follows:

SWD pins	Debug Function	Pin definition
SWDIO	SWD Data Input/Output	PG9
SWCLK	SWD Clock Input	PG8

Note: *Both PG9 and PG8 pins are default to be input state after chip reset, unlike most GPIOs.*

3.2.2 Pull-up Resistance

After chip reset, the SWDIO pin enables the internal pull-up (~ 100K ohm) by default, the SWCLK pin does not enable the internal pull-up resistor by default, so users need to connect external pull-up resistors or enable pull-up resistors by software on the PCB to prevent the floating of the input pin from causing increased leakage.

3.3 SW Interface Protocol

3.3.1 SW Protocol Introduction

SWD protocol uses LSB-first for data sending and receiving. Through the SWD interface, the debug master can read and write DPACC and APACC register sets.

SWIO needs to insert turn-around time on the bus each time the data direction is switched, and neither the host nor the slave will drive SWIO during this time. Between two transmissions, the host must drive the line low to enter the idle state, or continue to send the start bit of a new transmission to continue transmission. after a packet transmission, the host can also be idle to keep the line high or The SWD protocol does not have an explicit reset signal, and the host or target will detect a reset when it does not see the expected signal. By holding the line high for 50 clock cycles followed by a request to read the ID, a successful resynchronization can be ensured after an error or reset is detected.

3.3.2 SW Protocol sequence

Each SWD communication transmission sequence consists of three parts.

1. Packet request (8bits), sent by the host
2. ACK response (3bits), sent back by the target
3. Data transfer phase (33bits), sent by the host or target

where the packet request byte is defined as follows:

Bit	Name	Description
0	Start	Start bit, must be 1
1	ApnDP	AP/DP select 0：DP access 1：AP access
2	RnW	Read/Write select 0：write request 1：read request

4:3	A[3:2]	Address field of DP/AP register
5	Parity	Check bits for Bit0~Bit4 data
6	Stop	0
7	Park	Host not drive， pull-up via bus，target reads as 1

After the packet request is sent, there is always a 1bit turn-around time on the bus.

The ACK response is defined as follows:

Bit	Name	Description
0:2	ACK	001：FAULT 010：WAIT 100：OK

If the host initiates a read operation, or if the ACK is WAIT or FAULT, a turn-around time must be inserted after the ACK.

The data transfer format is as follows:

Bit	Name	Description
0:31	Data	Data of Read or write
32	Parity	Parity bit of 32bit data

3.3.3 SW-DP ID code

The SW-DP of Cortex-M0 has a fixed ID code: 0x0BB11477

The SW-DP is inactive until the host reads the ID code.

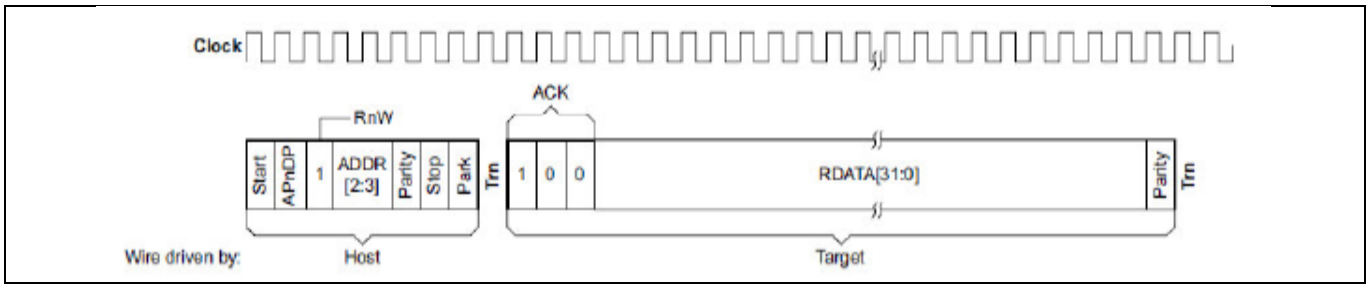
- SW-DP is in RESET state after chip reset, or after SWIO is pulled high for 50 SWCLK cycles
- After pulling SWIO low for at least 2 SWCLK cycles, SW-DP enters IDLE state
- When the SW-DP is in RESET, the host must first bring it into IDLE and then perform a read operation on the ID code register to activate the SW-DP. otherwise the slave will respond with a FAULT response to the host's communication.

3.3.4 Host Read

A successful read operation consists of the following three phases:

- An 8-bit read packet request from the host to the target.
- A 3-bit answer (ack) from the target to the host. A successful OK response is 100, a WAIT response is 010, and a FAULT response is 001.
- A 33-bit data read phase (payload) from the host to the target.

By default, there is a clocked turnaround period between the first and second phases and after the third phase, and a successful read operation is shown below.

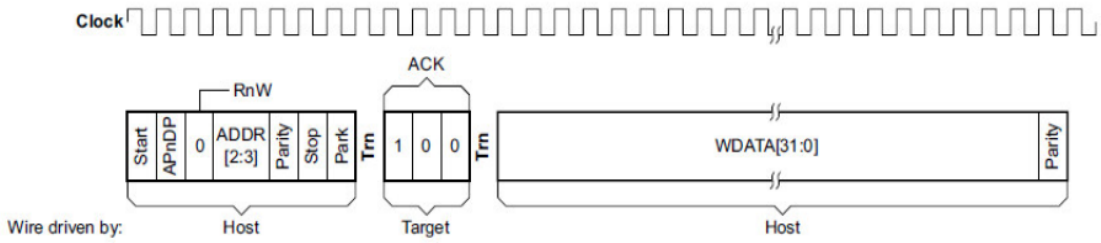


3.3.5 Host Write

A write operation consists of the following three phases

- An 8-bit write packet request (header) from the host to the target.
- A 3-bit answer (ack) from the target to the host. OK ack is 100 and FAULT ack is 001.
- A 33-bit data write phase (payload) from the host to the target.

By default, there is a clocked turnaround period between each two phases, and a successful write operation is shown below.



Revision history

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
1.1	2023.4			preliminary version

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