Shanghai Fudan Microelectronics Group Company Limited

复旦微电子

MG33A045EVB Advanced Smart Metering MCU

Brief Datasheet

2024.03

Contents

1 Product Overview

1.1 Introduction

MG33A045EVB is an low-power MCU with high-volume embedded memories and rich peripherals. MG33A045EVB integrates a 32-bit ARM Cortex-M0+ processor core with max frequency 64Mhz, up to 512K bytes Flash memory, up to 64K bytes RAM, and general peripherals including LCD, RTC, ADC, UART, I2C, SPI, Comparators, etc.

1.2 Block Diagram

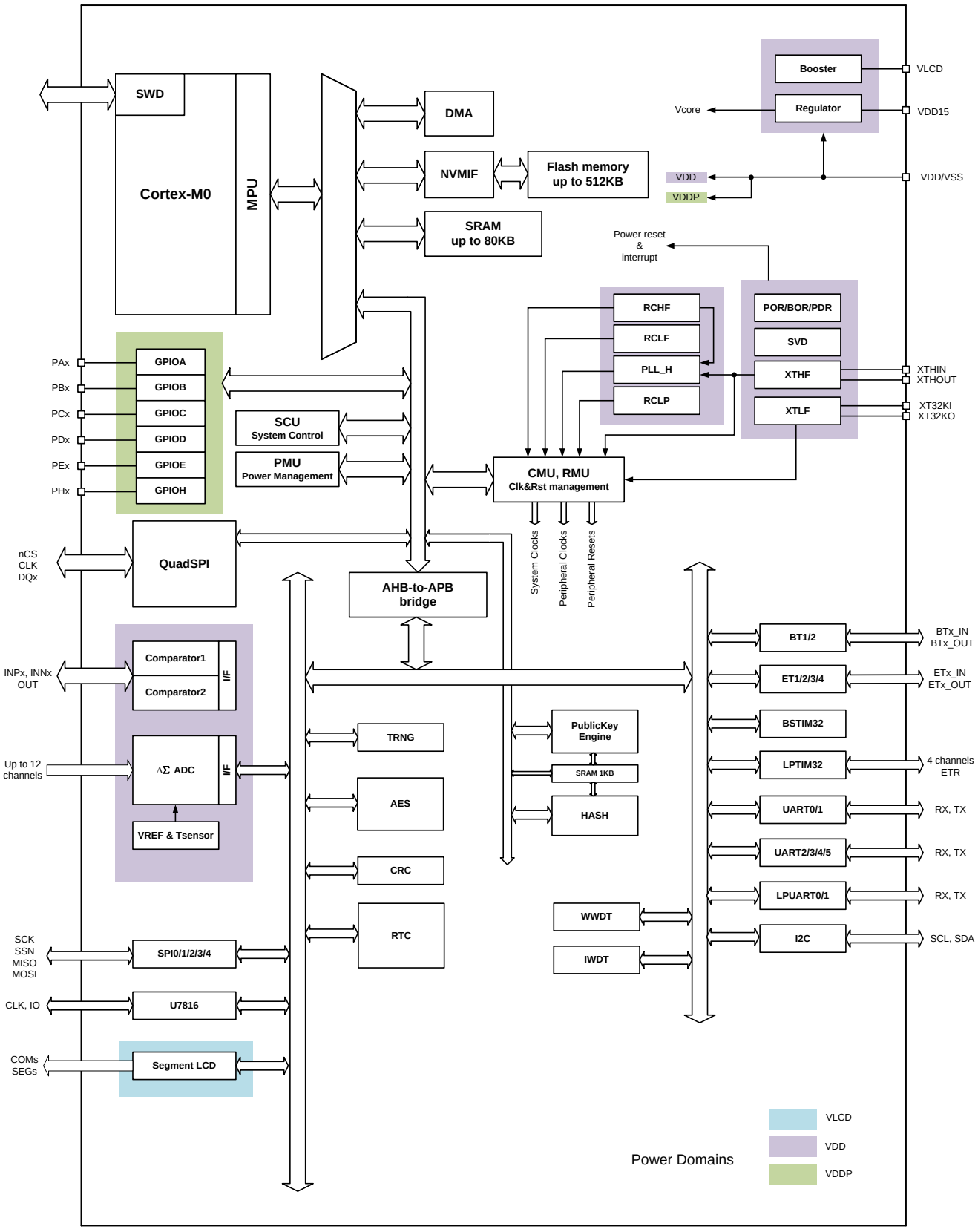


Figure 1-1 Block diagram

1.3 Features

- Operating Voltage Range: 1.8~5.5V
- Operating Temperature Range(Ambient): -40℃~+85℃
- Typical current consumption
  - Active：150uA/MHz
  - Sleep w/ LCD on：<10uA
  - DeepSleep w/ RTC & 16KB RAM：typ 2.5uA
- ARM Cortex-M0+
  - Frequency up to 64MHz
  - Memory Protection Unit
  - Unprivileged/Priviledged mode
  - Vector Table Offset Remapping
  - NVIC
  - SWD debug interface
- Memory
  - Up to 512K bytes embedded Flash
  - Flash endurance>20,000cycles
  - Bootloader self-progamming supported
  - Code protection mechanism
  - Up to 64K bytes RAM
- Rich analog
  - Software programmable Power-down reset & supply voltage monitor
  - 2x Low power comparators
  - Temperature Sensor
  - Sigma-Delta ADC w/ programmable OSR
- 24 external interrupt pins and 8 asynchronous wakeup pins
- 2 independent Watchdog timers
- Timer resources
  - 16bit extended timer*6
  - 32bit basic timer*1
  - 24-bit Systick*1
  - 32-bit low power timer*1
  - Windowed watchdog timer*1
  - Independent watchdog timer*1
  - RTCC with digital calibration, min step 0.06ppm
- Security features
  - AES128/192/256bit hardware accelerator, supporting ECB/CBC/CTR/GCM/GMAC

- Public Key accelerator: supporting ECC192/256/384, RSA2048
- HASH accelerator: supporting SHA-1 and SHA-256
- True Random Number generator

- Communication interface
  - UART*6
  - LPUART*2
  - 7816*1
  - I2C*2
  - SPI*5
  - 7-channel peripheral and 1-channel memory DMA
  - Programmable CRC module
- LCD driver
  - Up to 4COM×44SEG / 6COM×42SEG / 8COM×40SEG
  - Internal buffer mode or external capacitor mode
  - Support display under LPM
  - Internal VLCD voltage booster
  - 16-level of adjustable contrast
- Clocks
  - Programmable high speed RC oscillator, 8/16/24/32MHz, factory-trimmed to +/-0.5%, variation less than +/-2% for 8MHz under -40~+85℃
  - Low power 32K crystal oscillator w/ fail detector
  - On-chip low speed RC oscillator, 32KHz
  - PLL_L up to 16.384Mhz
  - PLL_H up to 72Mhz

1.4 Device Lineup

Part code	Flash（KBytes）	RAM（KBytes）	Package
MG33A045EVB	256	48	LQFP48

Table 1-1 MG33A045EVB device lineup

1.5 Electrical Characteristics

1.5.1 Limited parameters

Symbol	description	value	unit
V_{DD}	Power supply	-0.3 ~ 5.5	V
V_{PIN}	Pin voltage	V_{SS}-0.3 ~ V_{DD}+0.3	V
T_A	Operating temperature	-40 ~ 85	℃
T_{STG}	Storage temperature	-55 ~ 150	℃
HBM	ESD HBM	+/-4000	V
CDM	ESD CDM	+/-1000	V

Table 1-2 MG33A045EVB limited parameters

1.5.2 AC parameters

1.5.2.1 Security function performance

Symbol	description	condition	parameter			unit
			min	typ	max	
T_{sign}	ECDSA p256	F_{AHB}=40Mhz, estimated		12.6		ms
	ECDSA p384			39.3		ms
T_{verify}	ECDSA p256			54.6		ms
	ECDSA p384			171		ms
$T_{exchange}$	ECDH p256			53		ms
	ECDH p384			160		ms
T_{GCM}	AES-GCM-128	F_{APB}=40Mhz, estimated		180		us
	AES-GCM-256			200		us
T_{HASH}	SHA-256, 64bytes	F_{APB}=40Mhz, estimated		40		us

Table 1-3 MG33A045EVB Security Acceleration Estimated Performance

1.5.3 DC parameters

1.5.3.1 Operating conditions

Symbol	description	condition	Parameter			unit
			min	typ	max	
V_{DD}	Power supply		1.8		5.5	V
f_{HCLK}	AHB clock	-			64	Mhz
f_{PCLK}	APB clock	-			64	
T_J	Junction Temperature	T_A=-40~+85C	-40		105	° C

Table 1-4 MG33A045EVB supply parameters

1.5.3.2 Current consumption

Default condition: VDD=3.0V，T=25℃

Symbol	decription	condition	Parameter			Unit
			min	typ	max	
I_{sleep2}	Current consumption under SLEEP mode	PDR/LVD enabled, LCD disabled, RTC operating on 32K crystal, CPU & 64KB RAM state retained		4		uA
$I_{dpsleep}$	Current consumption under DEEPSLEEP mode	PDR/ LVD enabled, LCD disabled, RTC operating on 32K crystal, CPU & 16KB RAM state retained		2.5		μA
I_{VDD3}	Current consumption under ACTIVE mode	code excuting from Flash@24MHz		3.5		mA

Table 1-5 MG33A045EVB current consumption

1.5.3.3 Reset

Symbol	decription	condition		Parameter			Unit
				min	typ	max	
V_{POR}	Power-on reset voltage				1.8		V
V_{BOR}	Power-down reset voltage				1.7		V
V_{LVD}	Supply monitor threshold	LVD[3:0]=0000	Fall		1.800		V
			Rise		1.900		
		LVD[3:0]=0001	Fall		2.014		V
			Rise		2.114		
		LVD[3:0]=0010	Fall		2.229		V
			Rise		2.329		
		LVD[3:0]=0011	Fall		2.443		V
			Rise		2.543		
		LVD[3:0]=0100	Fall		2.657		V
			Rise		2.757		
		LVD[3:0]=0101	Fall		2.871		V
			Rise		2.971		
		LVD[3:0]=0110	Fall		3.086		V
			Rise		3.186		
		LVD[3:0]=0111	Fall		3.300		V
			Rise		3.400		
		LVD[3:0]=1000	Fall		3.514		V
			Rise		3.614		
		LVD[3:0]=1001	Fall		3.729		V
			Rise		3.829		
		LVD[3:0]=1010	Fall		3.943		V
			Rise		4.043		
		LVD[3:0]=1011	Fall		4.157		V

Symbol	decription	condition		Parameter			Unit
				min	typ	max	
			Rise		4.257		
		LVD[3:0]=1100	Fall		4.371		V
			Rise		4.471		
		LVD[3:0]=1101	Fall		4.586		V
			Rise		4.686		
		LVD[3:0]=1110	Fall		4.800		V
			Rise		4.900		

Table 1-6 MG33A045EVB Reset parameters

1.5.3.4 Internal RC oscillator

Symbol	description	condition		Parameter			unit
				min	typ	max	
f_{RCHF}[1]	RCHF frequency	VDD=5V	FSEL==2'b00	7.92	8	8.08	MHz
			FSEL==2'b01	15.84	16	16.16	
			FSEL==2'b10	23.76	24	24.24	
ACC_{RCHF}[2]	RCHF temperature variation	VDD=5V	FSEL==2'b00 T=-40~+85℃	-1	-	1.5	%
			FSEL==2'b01 T=-40~+85℃	-2.5	-	3	%
			FSEL==2'b10 T=-40~+85℃	-3	-	4	%
f_{RCLP}	RCLP frequency	VDD=1.8~5.5V T=25℃		28	32	35	KHz

Table 1-7 MG33A045EVB internal RC oscillation

1.5.3.5 ADC

symbol	description	condition	Parameter			Unit
			min	typ	max	
Reso	Resolution			13		bits
DNL	Differential nonlinearity			±1		LSB
INL	Integral nonlinearity		-2	±4	+5	
Offset			-12	±2	-8	
V_{IN}	Input voltage range		0		4.92	V
F_{ADC}	ADC operating clock			0.5	1	MHz
OSR	Over sampling rate		32	256	1024	
F_S	Throughput Rate			4K	32K	SPS

Table 1-8 MG33A045EVB ADC parameter

1.5.3.6 Temperature sensor

Symbol	description	condition	parameter			unit
			min	typ	max	
Reso		T_A=-40~+85C		±0.05		°C

Symbol	description	condition	parameter			unit
			min	typ	max	
Slope				TBD		LSB/°C

Table 1-9 MG33A045EVB TS parameter

1.5.3.7 Flash

Symbol	description	condition	parameter			unit
			min	typ	max	
	Flash size			-	512K	bytes
	Page size			512		bytes
	Sector size			2K		bytes
T_{PROG}	Word Program Time			25		μs
T_{ERASE}	Sector/Page Erase			2		ms
	Chip Erase			8		ms
N_{ED}	Sector Endurance			100,000		cycles

Table 1-10 MG33A045EVB Flash Characteristics

2 Pinout

2.1 LQFP48

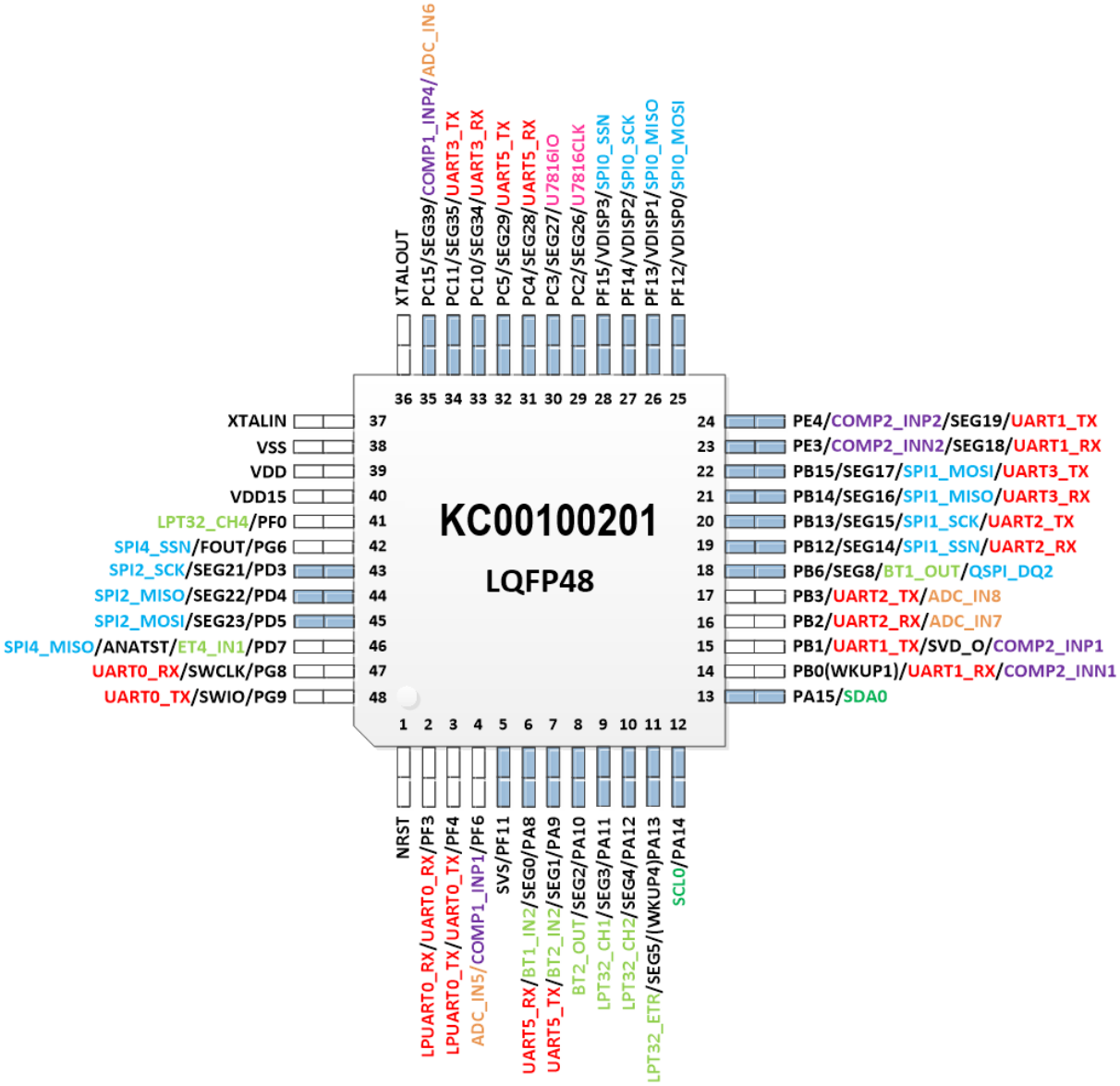


Figure 2-1 LQFP48 pin-out

3 Package

3.1 LQFP48

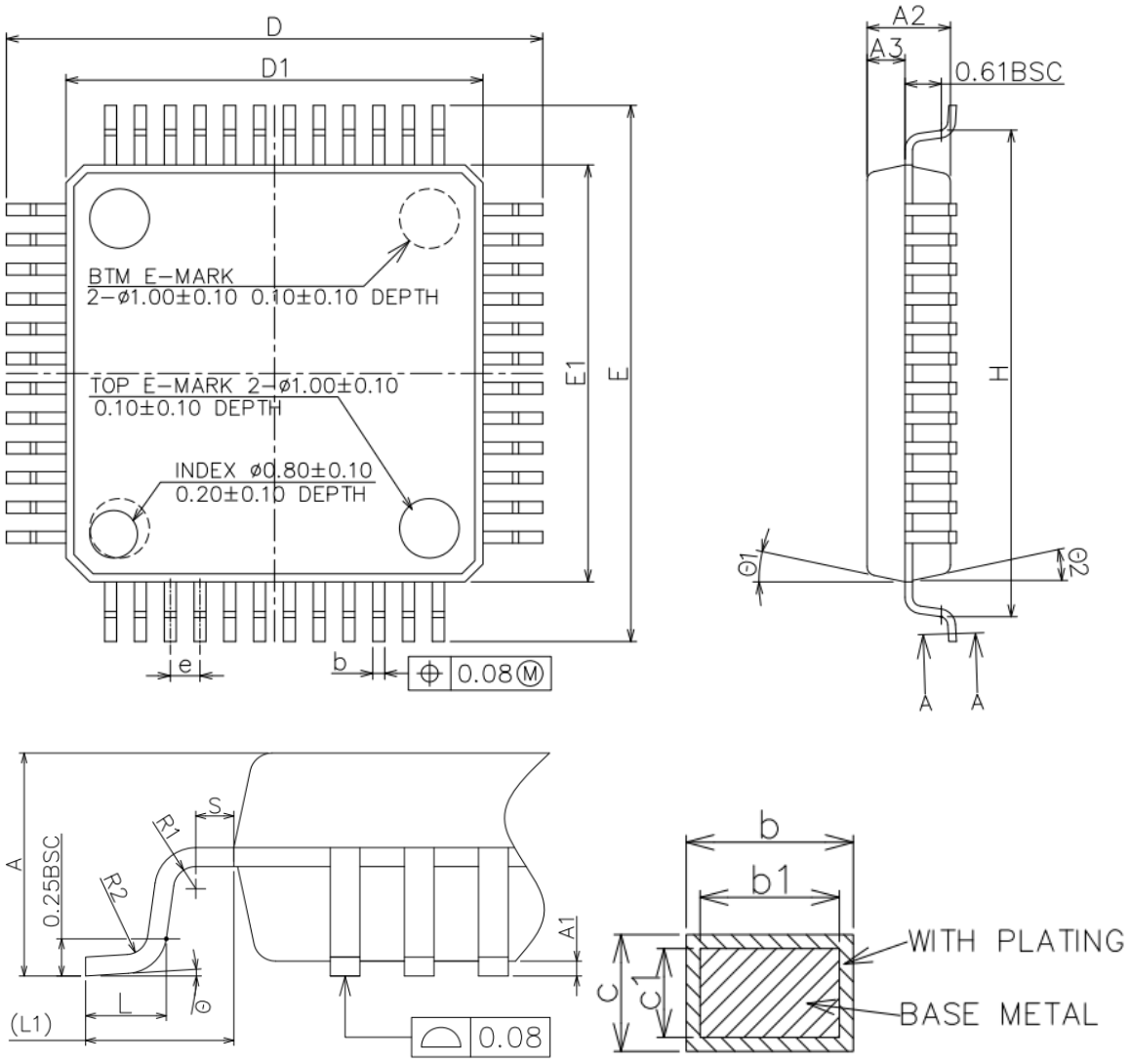


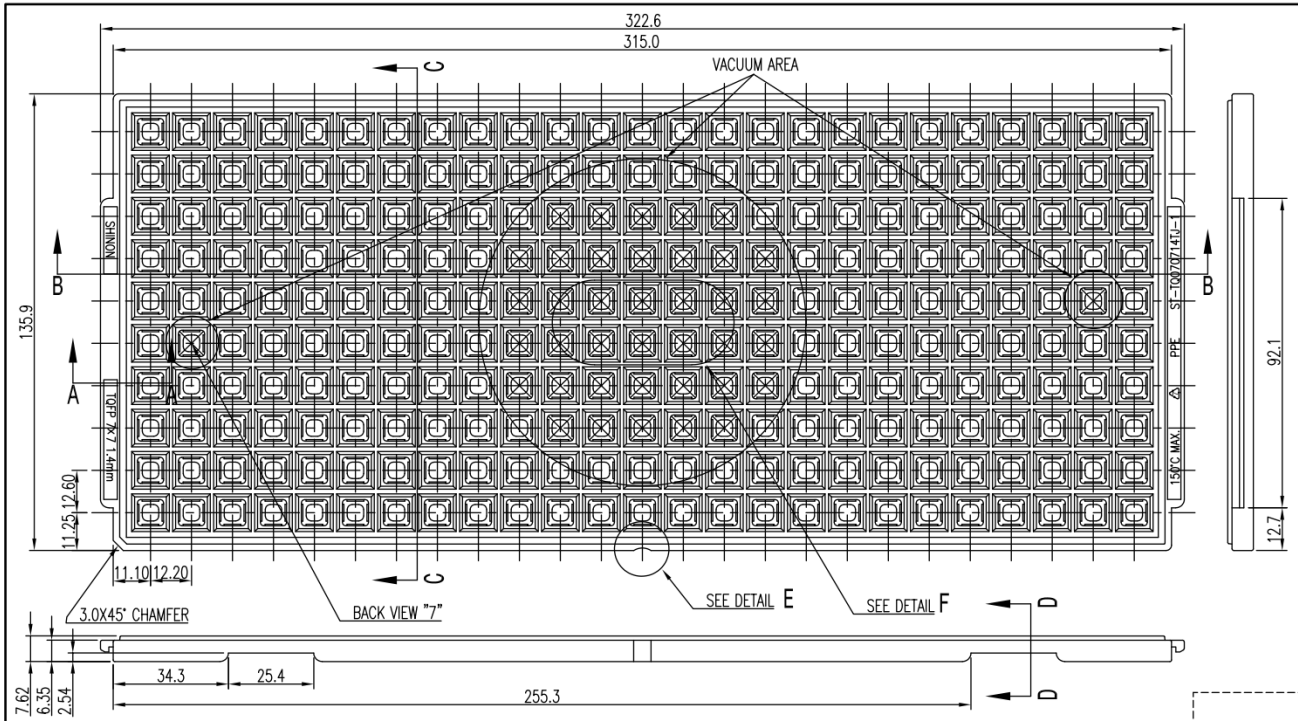
图 3-1LQFP48 封装尺寸图

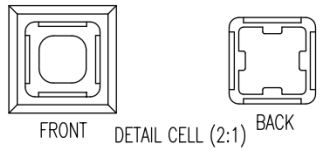
Symbol	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27

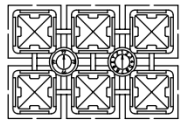
Symbol	MIN	NOM	MAX
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.50BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTE:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026BDD.

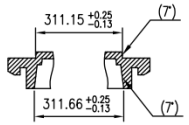
Figure 3-2 LQFP48 package information



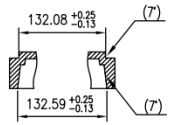




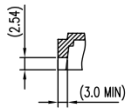
DETAIL F BACK VIEW DATE MARK(1:1)



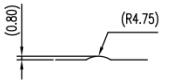
SECTION B–B (1:1)



SECTION C–C (1:1)

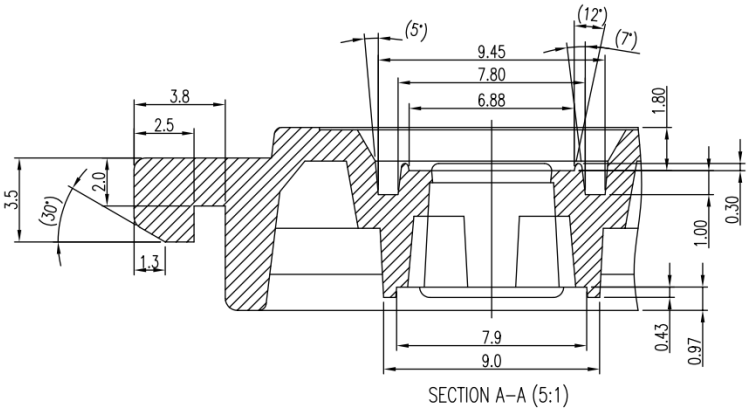


SECTION D–D (1:1)



NOTE: SCALLOP IS CENTERED ON SIDE OF TRAY.

DETAIL E (1:1)



SECTION A–A (5:1)

TRAY PURCHASING INFORMATION

*VENDOR & TRAY DESIGNATOR

SHINON | TQFP 7×7 1.4mm

*TEMPERATURE RATING & RECYCLE MARK & MATERIAL & PART NUMBER

150°C MAX. | PPE | ST-TQ070714TJ-1

NOTES

1.SURFACE ELECTRIC RESISTIVITY: $1\times10^{5}\sim9\times10^{9}\,\Omega/\square$. (BY TEST ASTM D257)
2.WARPAGE IS WITHN 0.76mm.
3.THE NUMERICAL VALUE IN PARENTHESES IS REFERENCE VALUE.

REVISONS				TITLE LQFP 7x7x1.4mm JEDEC TRAY	DATE 2010/10/18
ITEM	DESCRIPTION	DATE	DRAWN	PART NO. ST-TQ070714TJ-1 (7)	REV. 00
				DRAWING NO. EH-01220	REF.# 00674
				SCALE 7:10 UNIT mm CHECKED BY	DESIGNED BY F.Guan
				TOLERANCE X.X=±0.25 X.XX=±0.13 APPROVED BY	THIRD ANGLE PROJECTION
				SHEET NO. 1/1	
				MATERIAL PPE 150°C MAX.	SHINON CORPORATION

4 Flash memory protection

Flash memory protection can be used to protect user code, user data and user configuration information in Flash from being read or tampered with by unauthorized third party. Flash Protection includes two types: DBRDP-Debug ReaD Protection and ACLOCK-Application Code Block Locking. Flash protection is controlled via OPTBYTES in LDT1.

4.1 Debug interface protection（DBRDP – DeBug Read Protection）

The primary purpose of DBRDP is to prevent unauthorized access to the Flash content through the Debug interface.
DBRDP is enabled or disabled by the OPTBYTES.DBRDPEN configuration word in LDT1 page (0xAA means DBRDP is disabled, which is default state of a fresh device).
There are two levels of DBRDP: basic protection and fuse protection

Disable DBRDP： no protection
Flash can be read, erased, and programmed through the SWD interface.

Basic protection level:
Flash main array cannot be read or erased or programmed via the SWD interface. How to exit basic protection: Perform full-space matrix erase through SWD. After matrix erase is completed, SWD can modify OPTBYTES to disable DBRDP, and then reset the chip. After reset the chip will be in no protection state.

Fuse protection:
Under fuse protection, the SWD is permanently disabled.This means FudanMicro is unable to perform any failure analysis on the chip. In the case of fuse protection, the Debugger cannot establish a connection with the CPU anymore.

4.2 ACLOCK – Application Code Lock

The main purpose of ACLOCK is to prevent any unauthorized reading or tampering to the application code in Flash from hacking code. With the ACLOCK function, you can set some part of flash as fetch-ony, any read-as-data or modifying are prohibited. ACLOCK works in the granularity of 8KB. The whole Flash contains 32 Blocks with 2bit LOCK information for each Block. The default LOCK word is 0xFFFF_FFFF for a fresh device, which is unprotected. When the corresponding LOCK bits are set to 01 or 10, this block can only be fetched by CPU. When the corresponding LOCK bits are 00, both CPU and SWD are prohibited to read or modify the block. ACLOCK function is disabled by default. The user needs to enable ACLOCK through the programmer, and the user code should conform to the ACLOCK configuration when compiling (for example, literal pool cannot be compiled to the locked Block).

Functions of ACLOCK：

- No protection： All blocks allow CPU to fetch, read, and modify. No restriction on SWD access.
- Read-write protection: specified blocks allow CPU to fetch only, read & modify by CPU and DMA is prohibited. No restriction on SWD access.
- Software and SWD protection: specified blocks allow CPU to fetch only, read & modify by CPU, DMA and SWD is prohibited.

The relationship between LOCK bit and Block access permissions is shown in the following table:

LOCK bit	CPU read	CPU fetch	SWD read and erase/program
11	√	√	√
01/10	×	√	√
00	×	√	

ACLOCK information is loaded into registers after system reset. These registers can also be set by software, but cannot be cleared by software (it is only possible for software to escalate the protection level).
LOCK register contents are invalid when ACLOCK is not enabled.

Note: *ACLOCK is independent of DBRDP for each Block in Flash. For SWD interfaces, DBRDP has higher priority than ACLOCK, that is, after DBRDP is enabled, SWD cannot access Flash regardless of whether ACLOCK is enabled or not.*

Exit ACLOCK: Full-space matrix erase must be performed by SWD. After matrix erasing, SWD can modify OPTBYTES to disable ACLOCK, and then reset the chip. After reset, ACLOCK is unactivated.

5 Debug Support

5.1 Introduction

The chip is based on the ARM Cortex-M0 processor and supports the corresponding debug features. Through hardware breakpoints (breakpoints) and data watchpoints (watchpoints), the debugger can stop the CPU core operation during specific instruction fetches and data accesses, inspect the core registers and system peripheral state, and resume the core operation as needed.

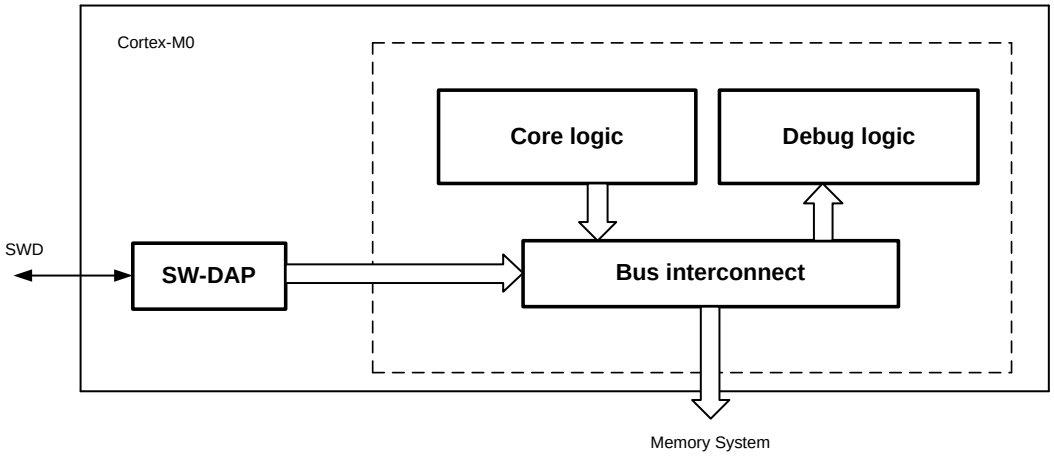


Figure 5-1 Cortex-M0 debug system diagram

For debug features of the Cortex-M0 core, please refer to the Cortex-M0 Technical Reference Manual from ARM.

5.2 Debug Pin

5.2.1 SWD Pin

The SWD pins of this chip are as follows:

SWD pins	Debug Function	Pin definition
SWDIO	SWD Data Input/Output	PG9
SWCLK	SWD Clock Input	PG8

Note: *Both PG9 and PG8 pins are default to be input state after chip reset, unlike most GPIOs.*

5.2.2 Pull-up Resistance

After chip reset, the SWDIO pin enables the internal pull-up (~ 100K ohm) by default, the SWCLK pin does not enable the internal pull-up resistor by default, so users need to connect external pull-up resistors or enable pull-up resistors by software on the PCB to prevent the floating of the input pin from causing increased leakage.

5.3 SW Interface Protocol

5.3.1 SW Protocol Introduction

SWD protocol uses LSB-first for data sending and receiving. Through the SWD interface, the debug master can read and write DPACC and APACC register sets.

SWIO needs to insert turn-around time on the bus each time the data direction is switched, and neither the host nor the slave will drive SWIO during this time. Between two transmissions, the host must drive the line low to enter the idle state, or continue to send the start bit of a new transmission to continue transmission. after a packet transmission, the host can also be idle to keep the line high or The SWD protocol does not have an explicit reset signal, and the host or target will detect a reset when it does not see the expected signal. By holding the line high for 50 clock cycles followed by a request to read the ID, a successful resynchronization can be ensured after an error or reset is detected.

5.3.2 SW Protocol sequence

Each SWD communication transmission sequence consists of three parts.

1. Packet request (8bits), sent by the host
2. ACK response (3bits), sent back by the target
3. Data transfer phase (33bits), sent by the host or target

where the packet request byte is defined as follows:

Bit	Name	Description
0	Start	Start bit, must be 1
1	ApnDP	AP/DP select 0：DP access 1：AP access
2	RnW	Read/Write select 0：write request 1：read request

4:3	A[3:2]	Address field of DP/AP register
5	Parity	Check bits for Bit0~Bit4 data
6	Stop	0
7	Park	Host not drive， pull-up via bus，target reads as 1

After the packet request is sent, there is always a 1bit turn-around time on the bus.

The ACK response is defined as follows:

Bit	**Name**	**Description**
0:2	ACK	001：FAULT 010：WAIT 100：OK

If the host initiates a read operation, or if the ACK is WAIT or FAULT, a turn-around time must be inserted after the ACK.

The data transfer format is as follows:

Bit	**Name**	**Description**
0:31	Data	Data of Read or write
32	Parity	Parity bit of 32bit data

5.3.3 SW-DP ID code

The SW-DP of Cortex-M0 has a fixed ID code: 0x0BB11477

The SW-DP is inactive until the host reads the ID code.

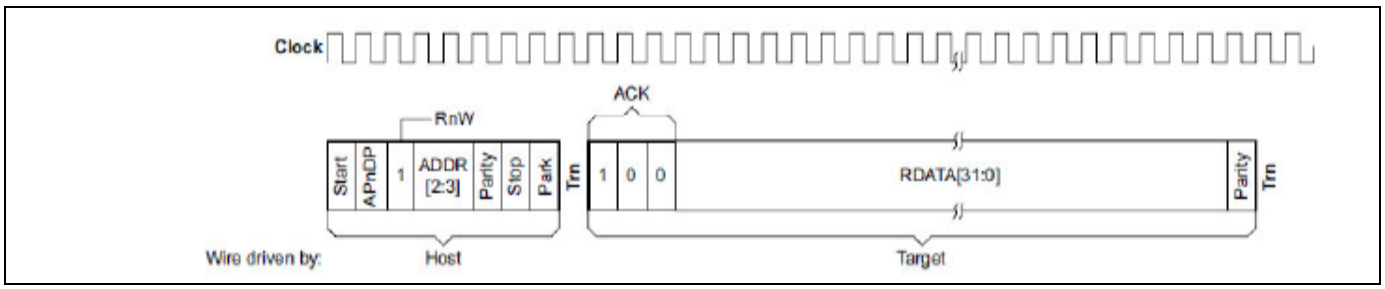
- SW-DP is in RESET state after chip reset, or after SWIO is pulled high for 50 SWCLK cycles
- After pulling SWIO low for at least 2 SWCLK cycles, SW-DP enters IDLE state
- When the SW-DP is in RESET, the host must first bring it into IDLE and then perform a read operation on the ID code register to activate the SW-DP. otherwise the slave will respond with a FAULT response to the host's communication.

5.3.4 Host Read

A successful read operation consists of the following three phases:

- An 8-bit read packet request from the host to the target.
- A 3-bit answer (ack) from the target to the host. A successful OK response is 100, a WAIT response is 010, and a FAULT response is 001.
- A 33-bit data read phase (payload) from the host to the target.

By default, there is a clocked turnaround period between the first and second phases and after the third phase, and a successful read operation is shown below.

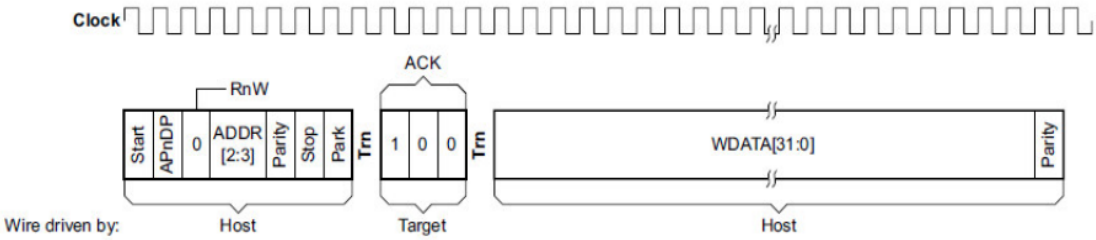


5.3.5 Host Write

A write operation consists of the following three phases:

- An 8-bit write packet request (header) from the host to the target.
- A 3-bit answer (ack) from the target to the host. OK ack is 100 and FAULT ack is 001.
- A 33-bit data write phase (payload) from the host to the target.

By default, there is a clocked turnaround period between each two phases, and a successful write operation is shown below.



Revision history

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
1.0	2024.03	14		Initial release
1.1	2024.10	21		Add debug description