



复旦微电子

FM24C02F/04F/08F
2-Wire Serial EEPROM
With Unique ID and Security Sector

Data Sheet

Aug. 2024



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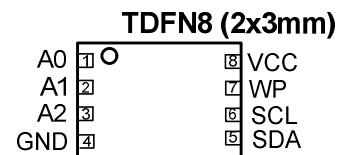
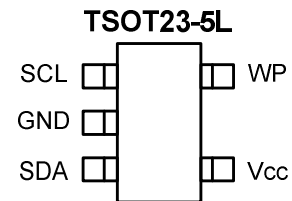
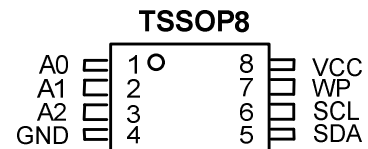
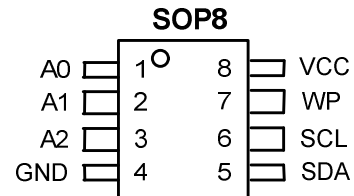
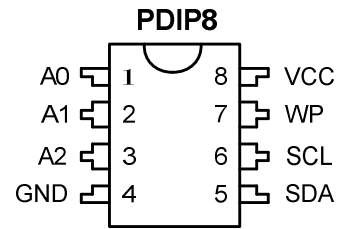
Description

The FM24C02F/04F/08F provides 2048/4096/8192 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 256/512/1024 words of 8 bits each, with 128-bit UID and 16-byte Security Sector. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential.

Features

- Low Operation Voltage: $V_{CC} = 1.7V$ to $5.5V$
- Internally Organized: 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K)
- 2-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bi-directional Data Transfer Protocol
- 400 kHz and 1MHz Compatibility
- Support Hardware and Software (SWP) Data Protection
- 16-Byte Page Write Modes (Partial Page Writes are Allowed)
- Lockable 16-Byte Security Sector
- 128-Bit Unique ID for each device
- Self-timed Write Cycle (5ms max)
- Operating Temperature range:
-40°C to +85°C
- High-reliability
 - Endurance: 1,000,000 Write Cycles
 - Data Retention: 100 Years
- PDIP8 (RoHS Compliant)
- SOP8, TSSOP8, TSOT23-5L and TDFN8 Packages (RoHS Compliant and Halogen-free)
- Wafer Sales: available in Wafer Form

Packaging Type



Absolute Maximum Ratings

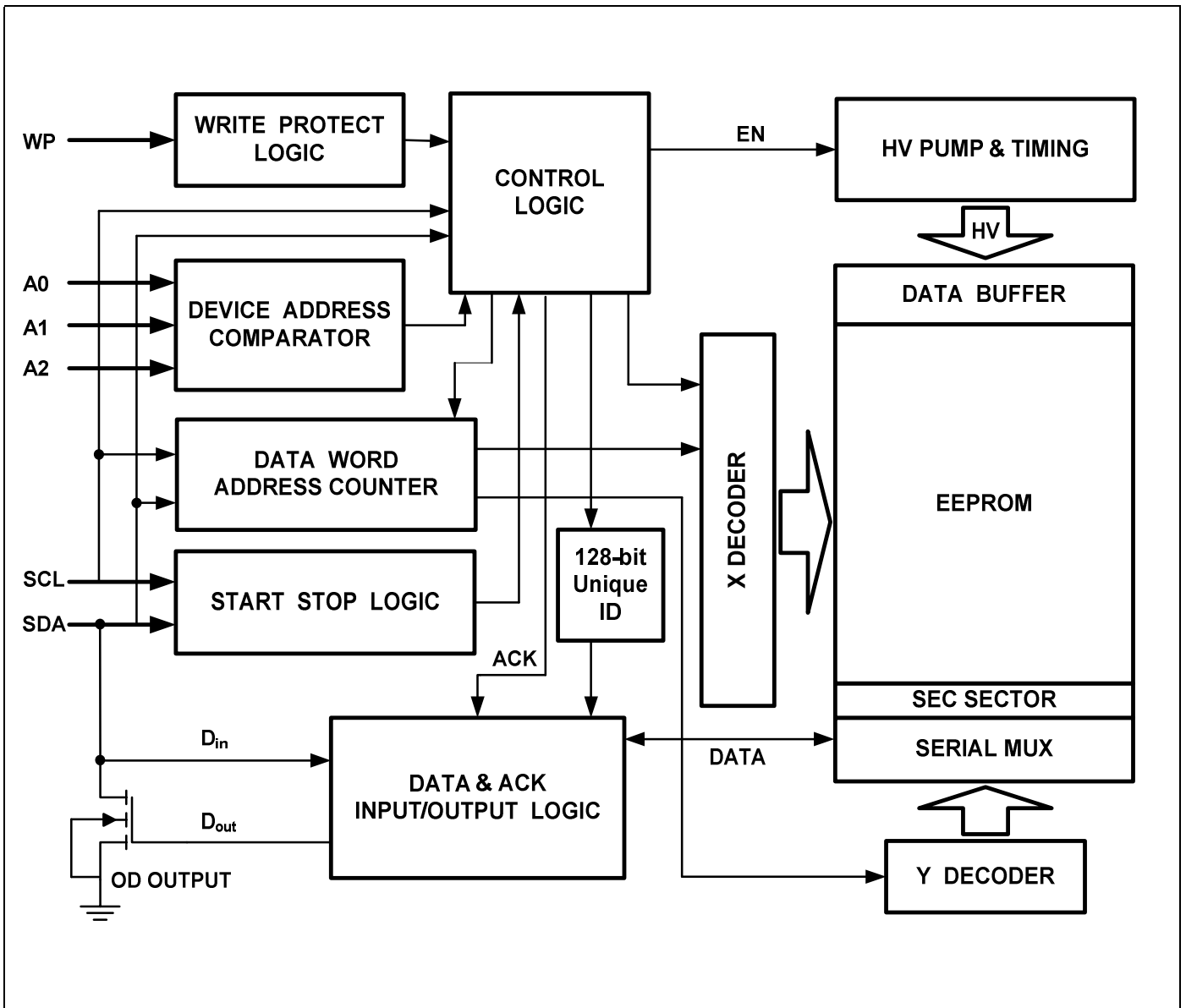
Ambient Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.5V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configurations

Pin Name	Function
A0~A2	Device Address Inputs
SDA	Serial Data Input/Output
SCL	Serial Clock Input
WP	Write Protect
V _{cc}	Power Supply
GND	Ground

Figure 1. Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired for the FM24C02F. As many as eight 2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The FM24C04F only uses the A2、A1 input for hardwire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pins are no connects.

The FM24C08F only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

WRITE PROTECT (WP): The FM24C02F/04F/08F has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to V_{CC} , the write protection feature is enabled.

Write Protect Description

In addition to hardware data protection (WP), the FM24C02F/04F/08F also provides software data protection (SWP) feature that will protect the memory against inadvertent writes. When SWP enabled, the whole memory will be read-only except SWP NVM bit. The SWP feature may be enabled (SWP=1'b) or disabled (SWP=0'b) by the user. The FM24C02F/04F/08F is shipped from FMSH with SWP disabled.

WP Pin and SWP bit Status	Part of the Array Protected		
	FM24C02F	FM 24C04F	FM 24C08F
WP= V_{CC}	Full (2K) Array and SWP bit	Full (4K) Array and SWP bit	Full (8K) Array and SWP bit
SWP=1	Full (2K) Array	Full (4K) Array	Full (8K) Array
WP=GND and SWP=0	Normal Read/Write Operations		

When the WP pin is connected to the V_{CC} , write operation to memory area is inhibited. When the WP pin is connected to GND or set in open, the write protect is invalid, and write operation in all memory area is available.

Write-protect condition: The WP pin must be connected to V_{CC} from start condition in the write operation (byte write, page write) until stop condition (refer to Figure 10).

If the WP pin changes during this time, the address data being written at this time is not guaranteed. Regarding the timing of write protect, refer to Figure 3.

Non-write-protect condition: The WP pin must be connected to GND from start condition in the write operation (byte write, page write) until the end of the internal write cycle ($t_{WR}(\max)=5ms$) (refer to Figure 11).

In not using the write protect, connect the WP pin to GND or set it open. The write protect is valid in the range of operation power supply voltage. As seen in Figure 10 when the write protect is valid, the EEPROM does not generate an acknowledgment signal after data input.



Memory Organization

FM24C02F, 2K SERIAL EEPROM: Internally organized with 16 pages of 16 bytes each, the 2K requires an 8-bit data word address for random word addressing.

FM24C04F 4K SERIAL EEPROM: Internally organized with 32 pages of 16 bytes each, the 4K requires an 9-bit data word address for random word addressing.

FM24C08F 8K SERIAL EEPROM: Internally organized with 64 pages of 16 bytes each, the 8K requires an 10-bit data word address for random word addressing.

Security Sector: The FM24C02F/04F/08F offers 16-byte Security Sectors which can be written and (later) permanently locked in Read-only mode. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

Unique ID: The FM24C02F/04F/08F utilizes a separate memory block containing a factory programmed 128-bit unique ID. Access to this memory location is obtained by beginning the device address word with a '1011'(Bh) sequence.

Memory Organization		
FM24C02F	FM 24C04F	FM 24C08F
Data Memory (16 X 16B)	Data Memory (32 X 16B)	Data Memory (64 X 16B)
Security Sector (1 X 16B)	Security Sector (1 X 16B)	Security Sector (1 X 16B)
Unique ID (1 X 16B)	Unique ID (1 X 16B)	Unique ID (1 X 16B)

Pin Capacitance

SYMBOL	PARAMETER	CONDITIONS	Max	Units
C_{IN}^1	Input Capacitance	$V_{IN} = 0V, f = 1MHz$	6	pF
C_{OUT}^1	Output Capacitance	$V_{OUT} = 0V, f = 1MHz$	8	pF

Note: 1. This parameter is characterized and is not 100% tested.



DC Characteristics

Applicable over recommended operating range from: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +1.7\text{V}$ to $+5.5\text{V}$, (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		1.7		5.5	V
I_{CC1}	Supply Current	$V_{CC} = 5.0\text{V}$, Read at 400KHz		0.2	0.5	mA
I_{CC2}	Supply Current	$V_{CC} = 5.0\text{V}$, Write at 400KHz		0.5	1.0	mA
I_{SB1}	Standby Current	$V_{CC} = 1.7\text{V}$, $V_{IN} = V_{CC}/V_{SS}$			1.0	μA
I_{SB2}	Standby Current	$V_{CC} = 5.5\text{V}$, $V_{IN} = V_{CC}/V_{SS}$			6.0	μA
I_{LI}	Input Leakage Current	$V_{IN} = V_{CC}/V_{SS}$		0.05	3.0	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}/V_{SS}$		0.05	3.0	μA
V_{IL}^1	Input Low Level		-0.45		$V_{CC} \times 0.3$	V
V_{IH}^1	Input High Level		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL2}	Output Low Level 2	$V_{CC} = 3.0\text{V}$, $I_{OL} = 2.1\text{ mA}$			0.4	V
V_{OL1}	Output Low Level 1	$V_{CC} = 1.7\text{V}$, $I_{OL} = 0.15\text{ mA}$			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

400 kHz AC characteristics

Recommended operating conditions: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +1.7\text{V}$ to $+5.5\text{V}$, $C_L = 100\text{ pF}$ (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency, SCL		400	kHz
t_{LOW}	Clock Pulse Width Low	1.3		μs
t_{HIGH}	Clock Pulse Width High	0.6		μs
t_I^1	Noise Suppression Time		80	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	μs
t_{BUF}^1	Time the bus must be free before a new transmission can Start	1.3		μs
$t_{HD.STA}$	Start Hold Time	0.6		μs
$t_{SU.STA}$	Start Setup Time	0.6		μs
$t_{HD.DAT}$	Data In Hold Time	0		μs
$t_{SU.DAT}$	Data In Setup Time	100		ns
t_R	Inputs Rise Time ¹		300	ns
t_F	Inputs Fall Time ¹		300	ns
$t_{SU.STO}$	Stop Setup Time	0.6		μs
t_{DH}	Data Out Hold Time	100		ns
t_{WS1}	WP setup time	1		μs
t_{WH1}	WP hold time	1		μs
t_{WS2}	WP release setup time	1		μs
t_{WH2}	WP release hold time	1		μs
t_{WR}	Write Cycle Time		5	ms
Endurance ¹	3.3V, 25°C, Page Mode	1,000,000		Write Cycles



1 MHz AC characteristics

Recommended operating conditions: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +1.7\text{V}$ to $+5.5\text{V}$, $CL = 100\text{ pF}$ (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency, SCL		1	MHz
t_{LOW}	Clock Pulse Width Low	500		ns
t_{HIGH}	Clock Pulse Width High	320		ns
t_i^1	Noise Suppression Time		80	ns
t_{AA}	Clock Low to Data Out Valid		450	ns
t_{BUF}^1	Time the bus must be free before a new transmission can Start	500		ns
$t_{HD.STA}$	Start Hold Time	250		ns
$t_{SU.STA}$	Start Setup Time	250		ns
$t_{HD.DAT}$	Data In Hold Time	0		ns
$t_{SU.DAT}$	Data In Setup Time	50		ns
t_R	Inputs Rise Time ¹		120	ns
t_F	Inputs Fall Time ¹		120	ns
$t_{SU.STO}$	Stop Setup Time	250		ns
t_{DH}	Data Out Hold Time	100		ns
t_{WS1}	WP setup time	1		μs
t_{WH1}	WP hold time	1		μs
t_{WS2}	WP release setup time	1		μs
t_{WH2}	WP release hold time	1		μs
t_{WR}	Write Cycle Time		5	ms
Endurance ¹	3.3V, 25°C, Page Mode	1,000,000		Write Cycles

Notes: 1. This parameter is characterized and is not 100% tested.

2. AC measurement conditions:

RL (connects to V_{CC}): 1.3 k Ω

Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}

Input rise and fall times: $\leq 50\text{ ns}$

Input and output timing reference voltages: 0.5 V_{CC}

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Figure 4). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Figure 5).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Figure 5).

ACKNOWLEDGE: All address and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

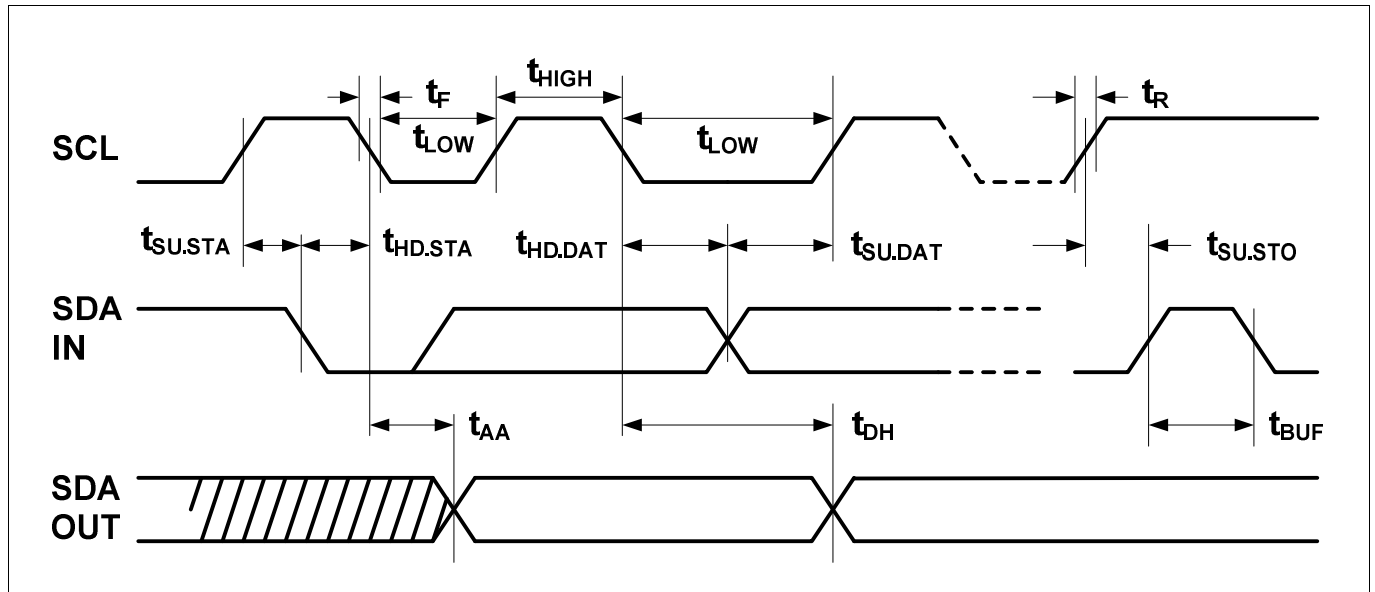
STANDBY MODE: The FM24C02F/04F/08F features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the stop bit and the completion of any internal operations.

Memory RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset in following these steps:

1. Clock up to 9 Cycles,
2. Look for SDA high in each cycle while SCL is high and then,
3. Create a start condition as SDA is high.

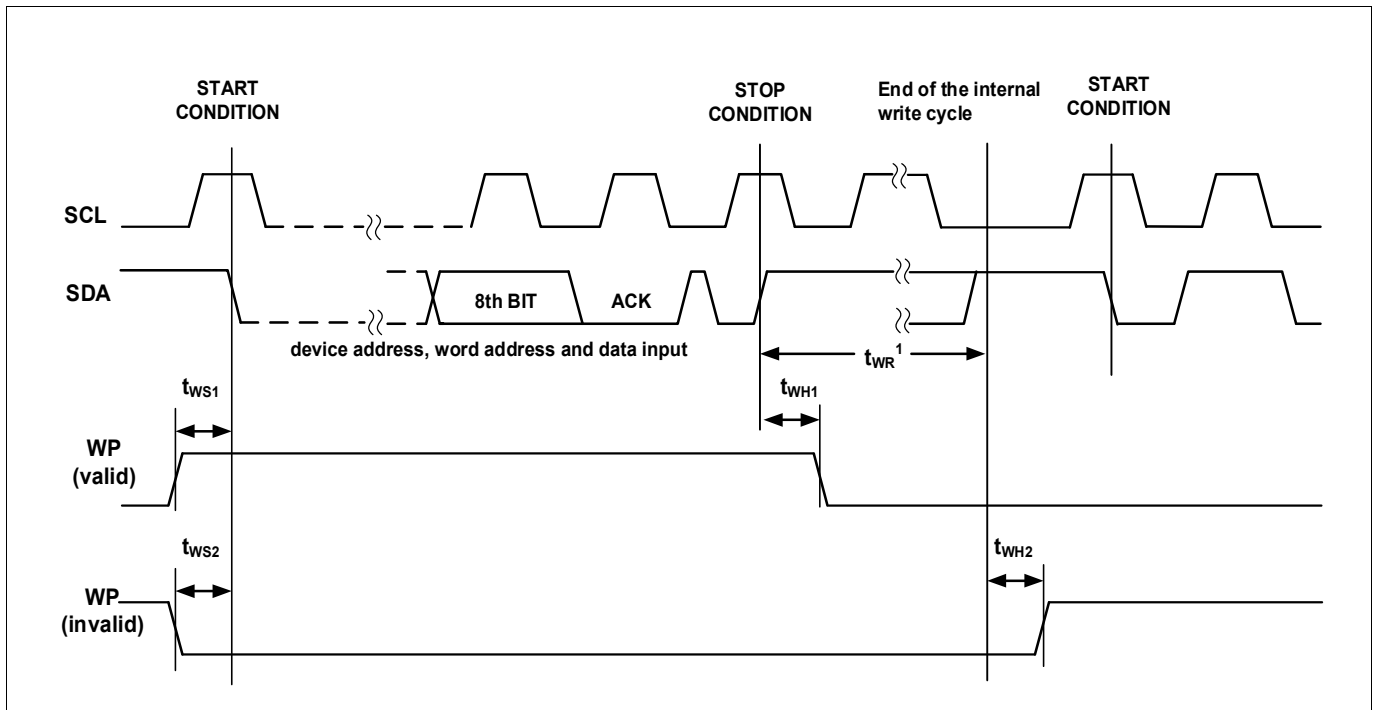
Bus Timing

Figure 2. SCL: Serial Clock, SDA: Serial Data I/O



Write Cycle Timing

Figure 3. SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 4. Data Validity

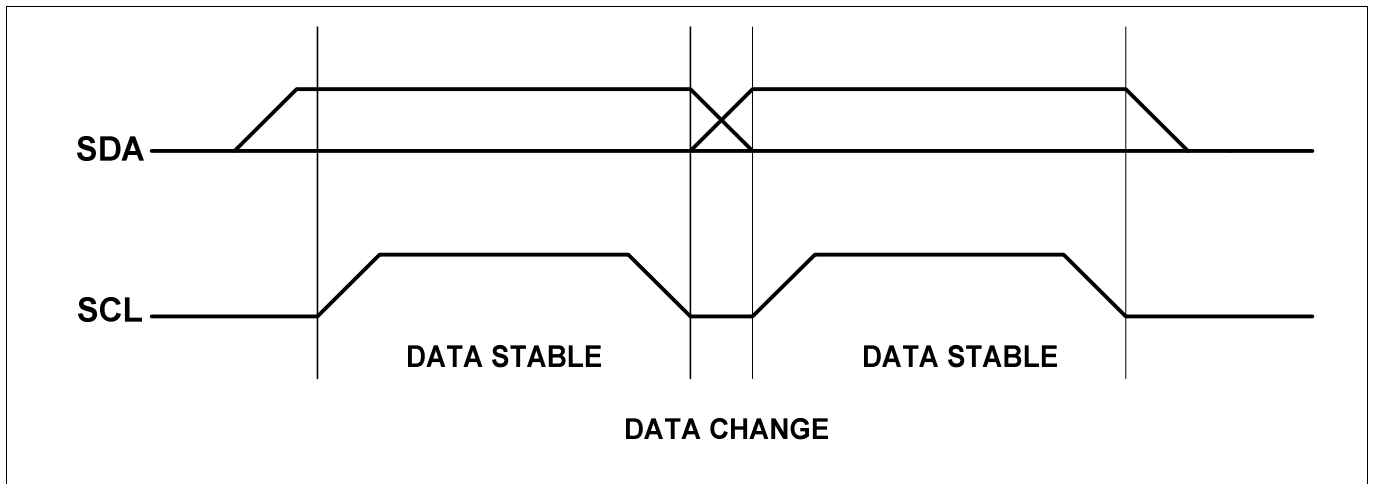


Figure 5. Start and Stop Definition

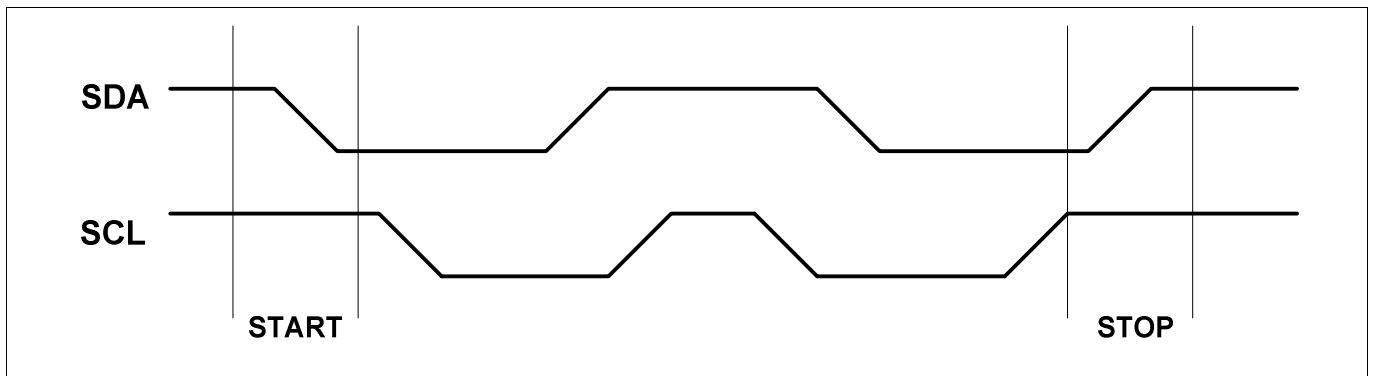
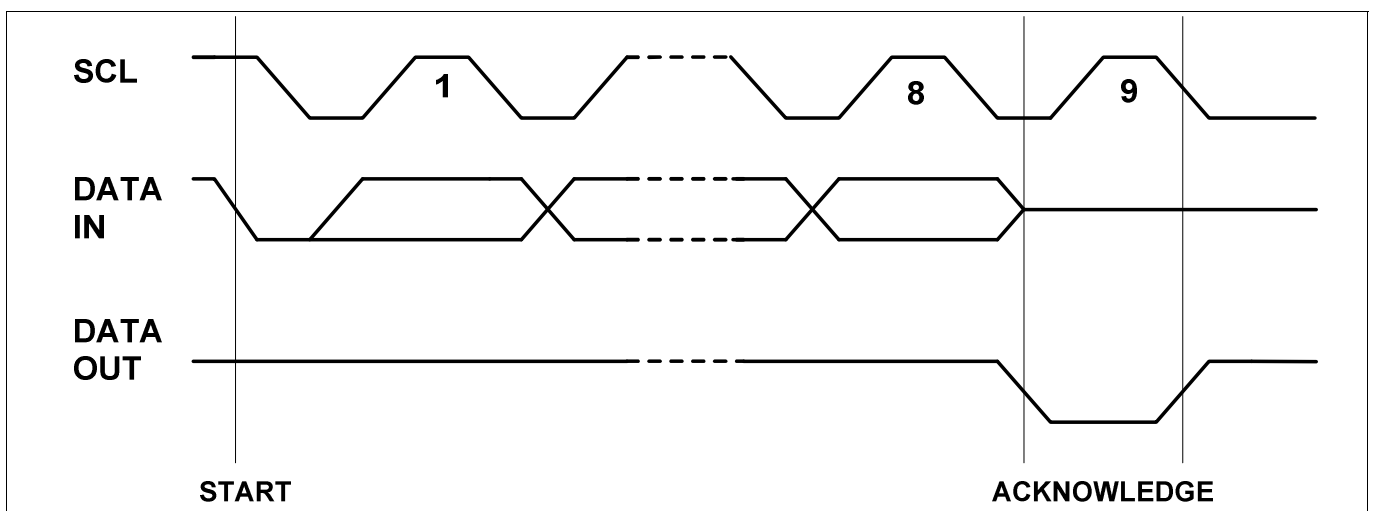
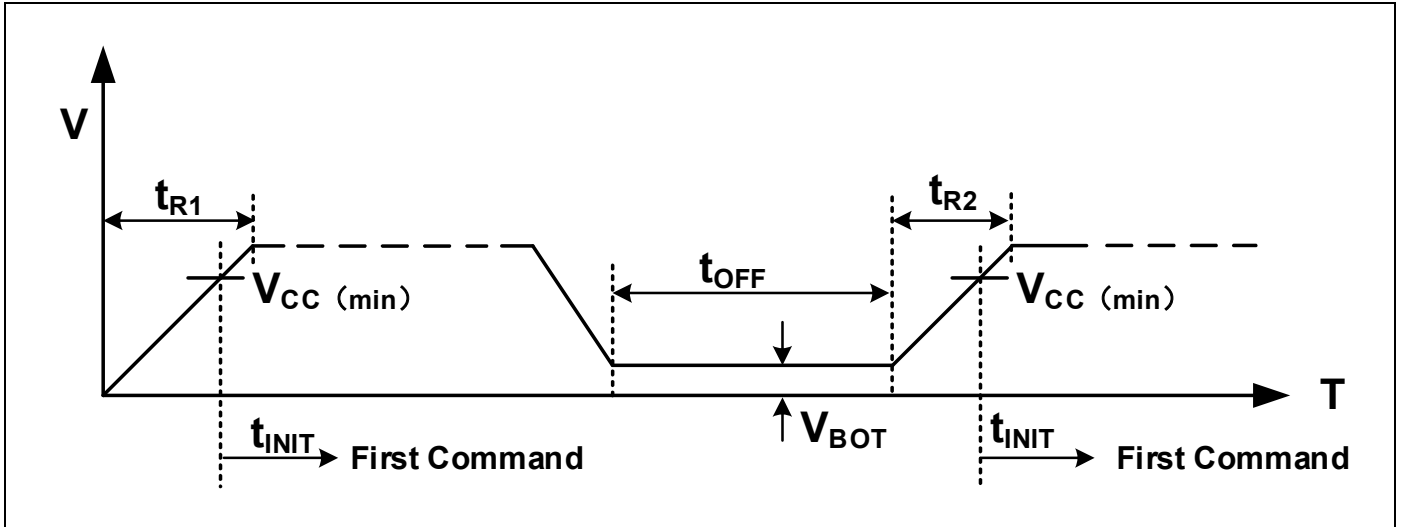


Figure 6. Output Acknowledge



Power-up Timing

Figure 7. V_{CC} Ramp Up and Ramp Down



Symbol	Parameter	Test Condition	Min	Max	Units
t_{R1}	Power on time from 0V			20	ms
t_{R2}	Power on time from V_{BOT}	$V_{BOT} \leq 0.2V$		5	ms
t_{OFF}	power cycle off time		50		ms
t_{INIT}	Time from power on to first command		100		us
V_{BOT}	Power Off threshold for the next power on cycle	No ringback above V_{BOT}		0.2	V

Note: V_{CC} must rise monotonically without ringback.

Device Addressing

Data Memory Access:

The FM24C02F/04F/08F device requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Table 1~Table 4).

The device address word consists of a mandatory '1010' sequence for the first four most significant bits as shown in Table 1~Table 4 on page 14. This is common to all the EEPROM devices.

The next 3 bits are the A2, A1 and A0 device address bits for the 2K EEPROM. These 3 bits must compare to their corresponding hard-wired input pins. The A2, A1 and A0 device address bits are "0" for the 2K EEPROM of TSOT23-5L package.

The 4K EEPROM only uses the A2, A1 for device addressing. The third bit is a memory page address bit(A[8]). The A2, A1 bit must compare to its corresponding hard-wired input pin. The A0 pin is no connecting.

The 8K EEPROM only uses the A2 device address bit with the next 2 bits(A[9:8]) being for memory page addressing. The A2 bit must compare to its corresponding hard-wired input pin. The A1 and A0 pins are no connecting.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state.

Unique ID Access: The FM24C02F/04F/08F utilizes a separate memory block containing a factory programmed 128-bit unique ID. Access to this memory location is obtained by beginning the device address word with a '1011'(Bh) sequence (refer to Table 1~Table 4). The behavior of the next three bits remains the same as during a standard memory addressing sequence.

The eighth bit of the device address needs be set to a one to read the Serial Number. Writing or altering the 128-bit unique ID is not possible.

For more details on accessing this special feature, See Read Operations on page 16.

Security Sector Access: The FM24C02F/04F/08F offers 16-byte Security Sector which can be written and (later) permanently locked in Read-only mode. Access to this memory location is obtained by beginning the device address word with a '1011'(Bh) sequence (refer to Table 1~Table 4). The behavior of the next three bits remains the same as during a standard memory addressing sequence.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

For more details on accessing this special feature, See Write Operations and Read Operations on page 15~16.

SWP Access: Access to this memory location is obtained by beginning the device address word with a '1011b'(Bh) sequence (refer to Table 1~Table 4). The behavior of the next three bits remains the same as during a standard memory addressing sequence.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

For more details on accessing this special feature, See Write Operations and Read Operations on page 15~16.

NOISE PROTECTION: Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device.

DATA SECURITY: The FM24C02F/04F/08F has provided Hardware and Software Data protection feature that will protect the memory against inadvertent writes, See Write Protect Description on page 5.

**Table 1. FM24C02F Device Address**

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	1	0	1	0	A2	A1	A0	R/W
Security Sector	1	0	1	1	A2	A1	A0	R/W
Security Sector Lock Bit	1	0	1	1	A2	A1	A0	R/W
Unique ID Number	1	0	1	1	A2	A1	A0	1
SWP	1	0	1	1	A2	A1	A0	R/W

MSB

LSB

Table 2. FM24C04F Device Address

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	1	0	1	0	A2	A1	A[8]	R/W
Security Sector	1	0	1	1	A2	A1	x	R/W
Security Sector Lock Bit	1	0	1	1	A2	A1	x	R/W
Unique ID Number	1	0	1	1	A2	A1	x	1
SWP	1	0	1	1	A2	A1	x	R/W

MSB

LSB

Table 3. FM24C08F Device Address

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	1	0	1	0	A2	A[9]	A[8]	R/W
Security Sector	1	0	1	1	A2	x	x	R/W
Security Sector Lock Bit	1	0	1	1	A2	x	x	R/W
Unique ID Number	1	0	1	1	A2	x	x	1
SWP	1	0	1	1	A2	x	x	R/W

MSB

LSB

Table 4. FM24C02F/04F/08F Word Address

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]
Security Sector	0	0	x	x	A[3]	A[2]	A[1]	A[0]
Security Sector Lock Bit	x	1	x	x	x	x	x	x
Unique ID Number	1	0	x	x	0	0	0	0
SWP	1	1	x	x	x	x	x	x

MSB

LSB

NOTE: 1. x = Don't care bit.**2. A[9:0] are Word Address.**

Write Operations

BYTE WRITE: A write operation requires two 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR} , to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 8).

PAGE WRITE: The EEPROM is capable of 16-byte page writes. A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 9).

The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

WRITE SECURITY SECTOR: Write the Security Sector is similar to the page write but requires use of device address, and the special word address seen in Table 1~Table 4 on page 14. Address bits A[7:6] which must be equal to ‘00b’. Lower address bits A[3:0] define the byte address inside the Security Sector (refer to Figure 15). And other address bits are don't care.

If the Security Sector is locked, the data bytes transferred during the Write Security Sector operation are not acknowledged (NoAck).

LOCK SECURITY SECTOR: Lock the Security Sector is similar to the byte write but requires use of device address, and special word address seen in Table 1~Table 4 on page 14. The word address bits A[7:6] must be ‘01b’, all other word address bits are don't care. The data byte must be equal to the binary value xxxx xx1x, where x is don't care (see Figure 16).

If the Security Sector is locked, the data bytes transferred during the Lock Security Sector operation are not acknowledged (NoAck).

WRITE SWP: Write SWP operation is similar to the byte write but requires use of device address, and specific word address seen in Table 1~Table 4 on page 14. The word address bits A[7:6] must be ‘11b’, all other word address bits are don't care. The data byte must be equal to the binary value ‘xxxx xxSWPx’ (see Table 5 and Figure 20).

Table 5. SWP NVM Bit

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
x	x	x	x	x	x	SWP	x

MSB LSB

NOTE: x = Don't care bit.

The SWP bit default value is ‘0b’ (SWP disabled). When Write SWP instruction has been sent, the next instruction issuing must wait for the end of the internal write cycle ($t_{WR}(\max)=5\text{ms}$), otherwise the instruction is invalid.



Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address “roll over” during read is from the last byte of the last memory page to the first byte of the first page. The address “roll over” during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (see Figure 12).

RANDOM READ: A random read requires a “dummy” byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see Figure 13).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 14)

UNIQUE ID READ: Reading the serial number is similar to the sequential read but requires use of the device address, a dummy write, and the use of specific word address seen in Table 1~Table 4 on page 14. Address bits A[7:6] which must be equal to ‘10b’. Lower address bits A[3:0] define the byte address inside the UID. And other address bits are don’t care. If the application desires to read the first byte of the UID, the lower address bits A[3:0] would need to be ‘0000b’.

When the end of the 128-bit UID number is reached (16 bytes of data), the data word address will roll-over back to the beginning of the 128-bit UID number. The Unique ID Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (see Figure 19).

READ SECURITY SECTOR: Read the Security Sector is similar to the random read but requires use of device address, a dummy write, and the use of specific word address seen in Table 1~Table 4 on page 14. The higher address bits are don’t care except for address bits A[7:6], which must be equal to ‘00b’. The lower address bits A[3:0] define the byte address inside the Security Sector.

The internal byte address is automatically incremented to the next byte address after each byte of data is clocked out. When the last byte (0Fh) is reached, it will roll over to 00h, the first byte of the Security Sector, and continue to increment. (see Figure 17).

READ LOCK STATUS: There are two ways to check the lock status of the Security Sector.

1. The first way is initiated by a Security Sector Write, the EEPROM will acknowledge if the Security Sector is unlocked, while it will not acknowledge if the Security Sector is locked.

Once the acknowledge bit is read, it is recommended to generate a Start condition followed by a Stop condition, so that:

- Start: the truncated command is not executed because the Start condition resets the device internal logic
- Stop: the device is then set back into Standby mode by the Stop condition.

2. The second way is initiated by a Lock Status Read. Lock Status Read is similar to the random read but requires use of device address seen in Table 1~Table 4, a dummy write, and the use of specific word address. The address bits A[7:6] must be ‘01b’, all other address bits are Don’t Care. The Lock bit is the BIT1 of the byte read on SDA. It is at “1” when the lock is active and at “0” when the lock is not active. The

same data is shifted out repeatedly until the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 18).

READ SWP: Read SWP operation is similar to the random read but requires use of device address, a dummy write, and specific word address. The address bits A[7:6] must be '11b', all other address bits are Don't Care. The SWP is the BIT1 of the byte read on SDA, other bits are '1b'. The internal byte address is not automatically incremented, so the same data is shifted out repeatedly until the microcontroller does not respond with a zero but does generate a following stop condition (see Figure 21).

Figure 8. Byte Write

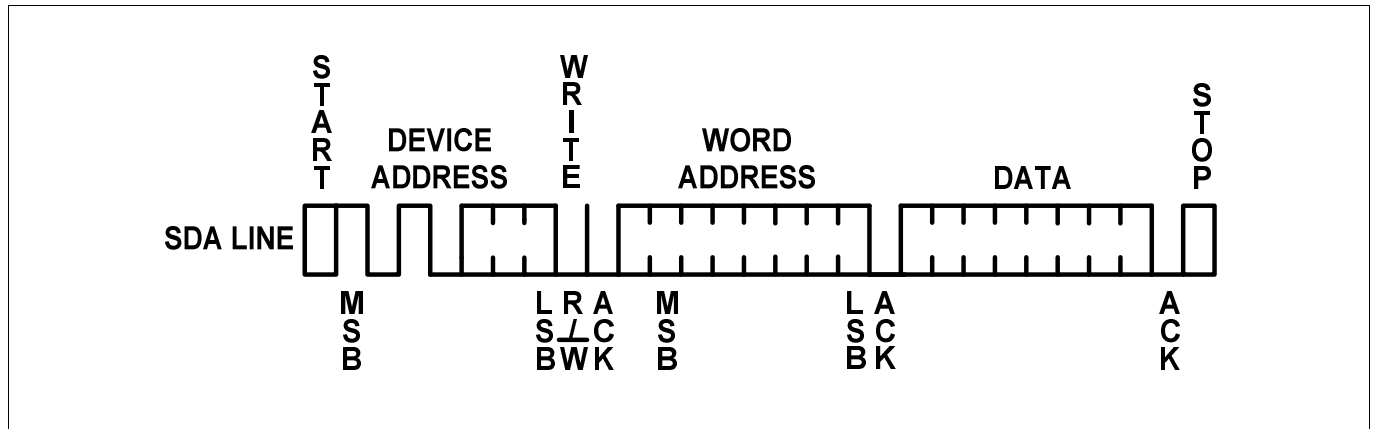


Figure 9. Page Write

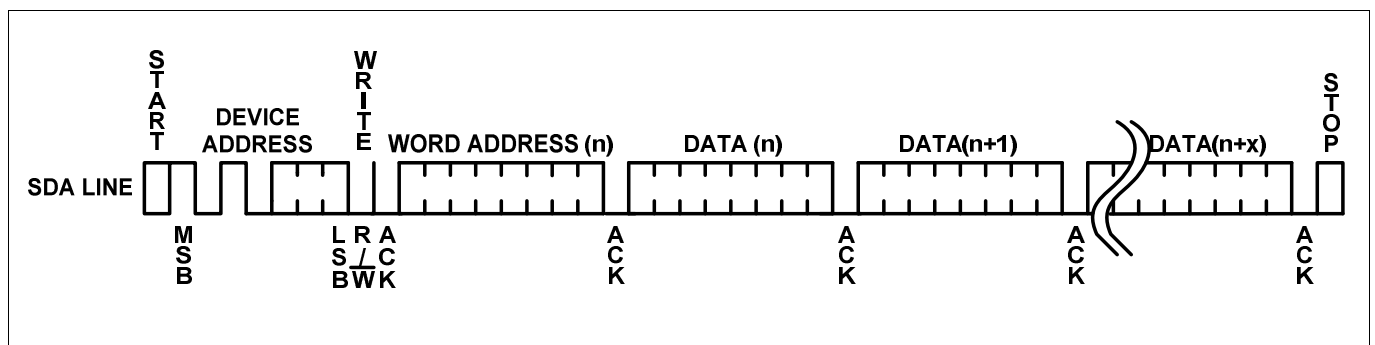


Figure 10. Write-Protect Condition

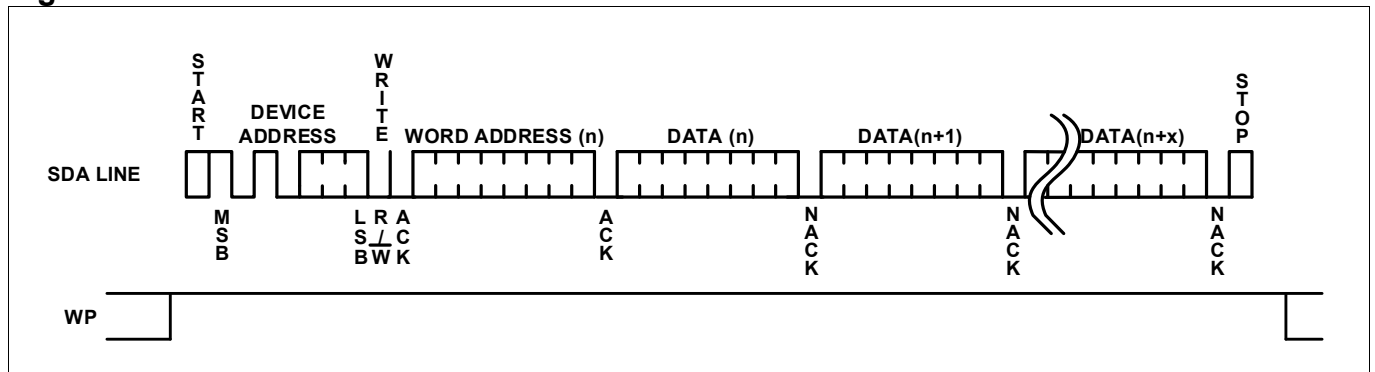


Figure 11. Non-Write-Protect Condition

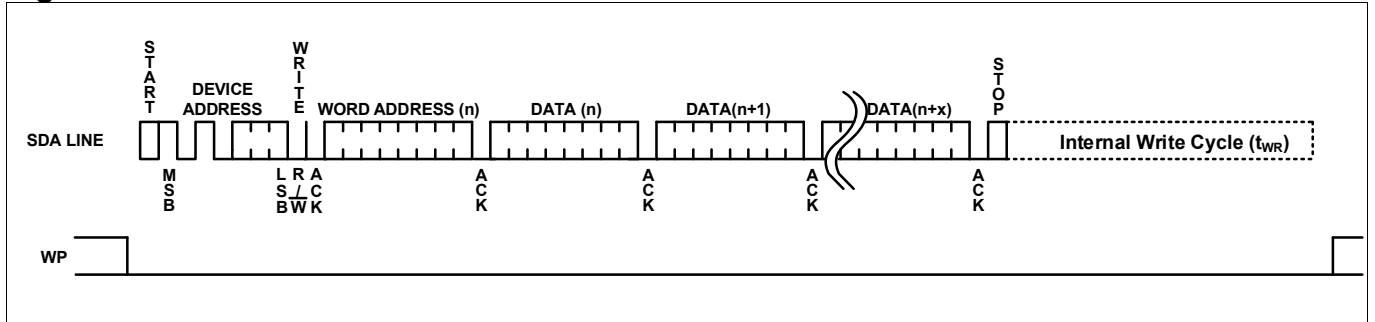


Figure 12. Current Address Read

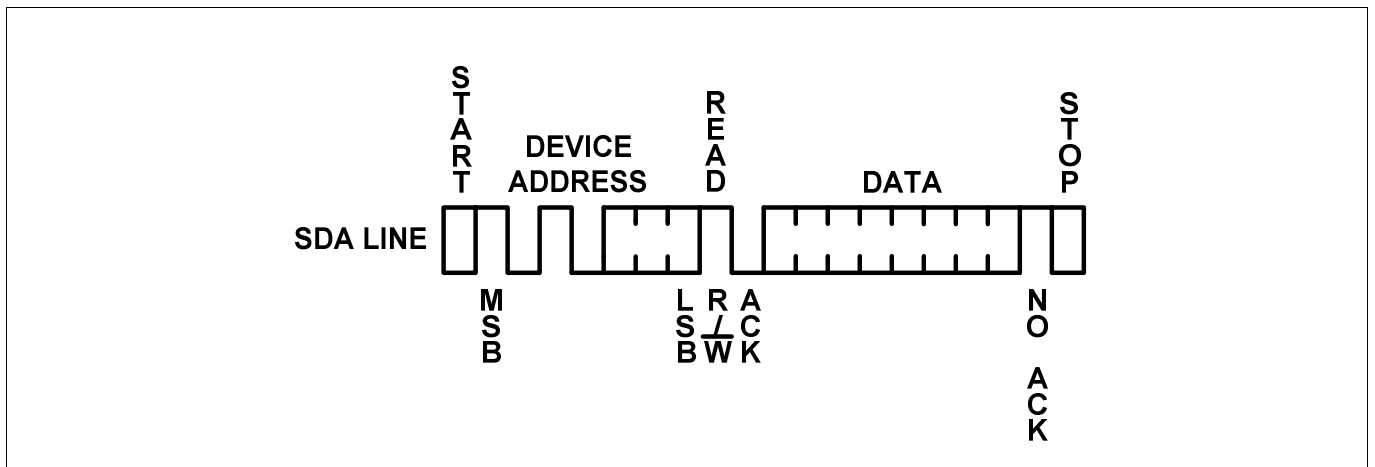


Figure 13. Random Read

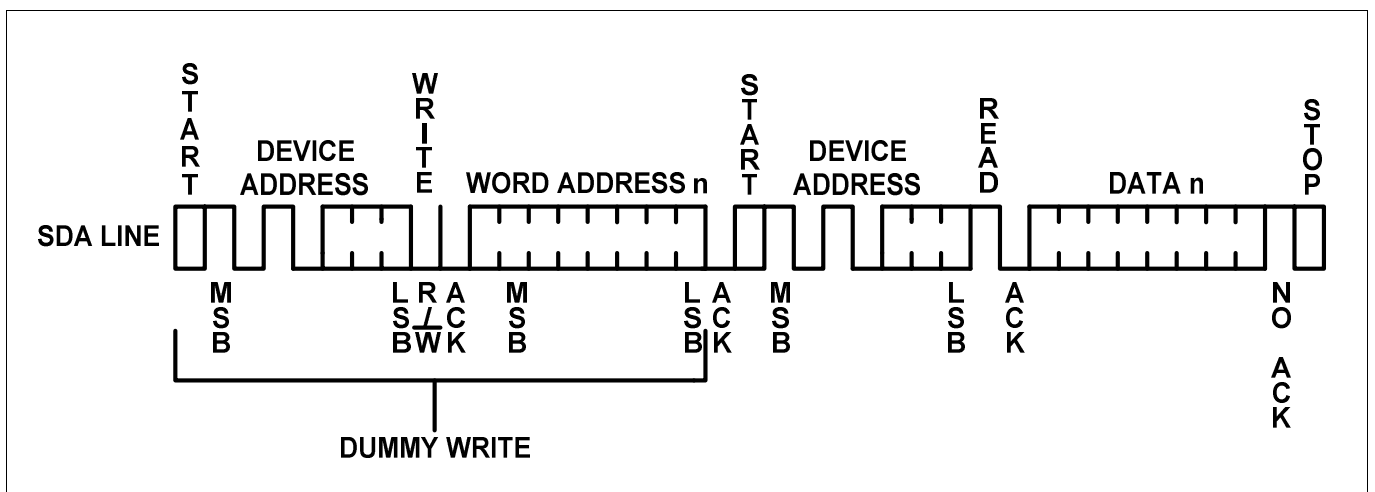


Figure 14. Sequential Read

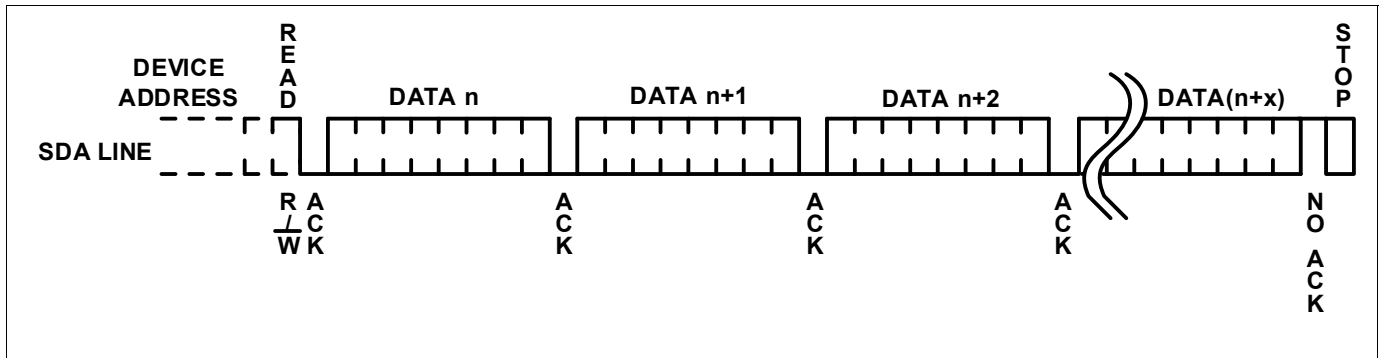


Figure 15. Write Security Sector

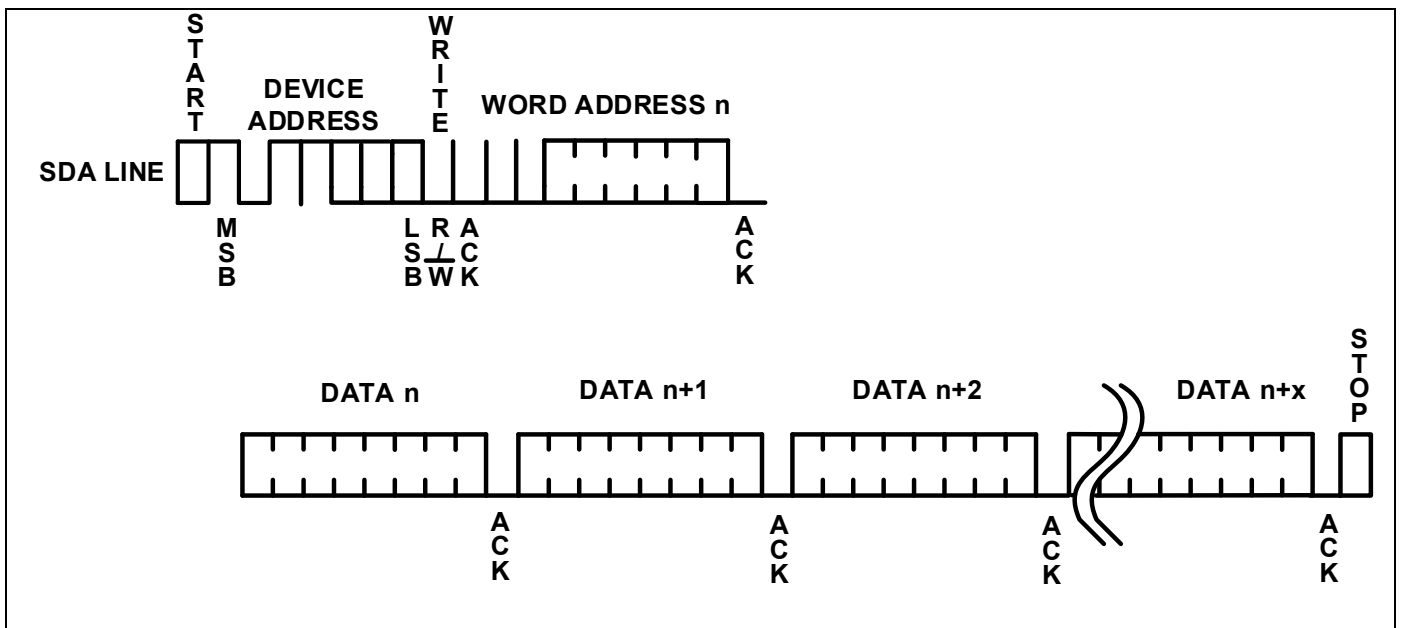


Figure 16. Lock Security Sector

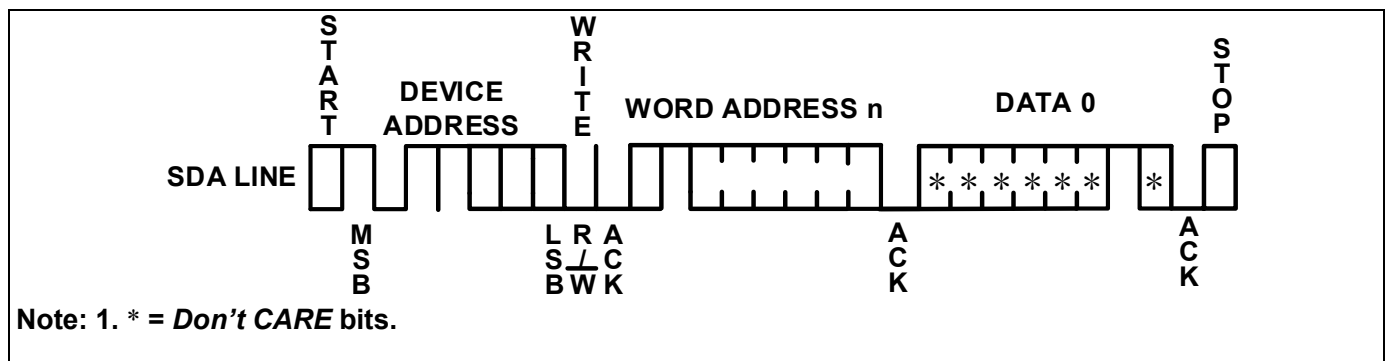


Figure 17. Read Security Sector

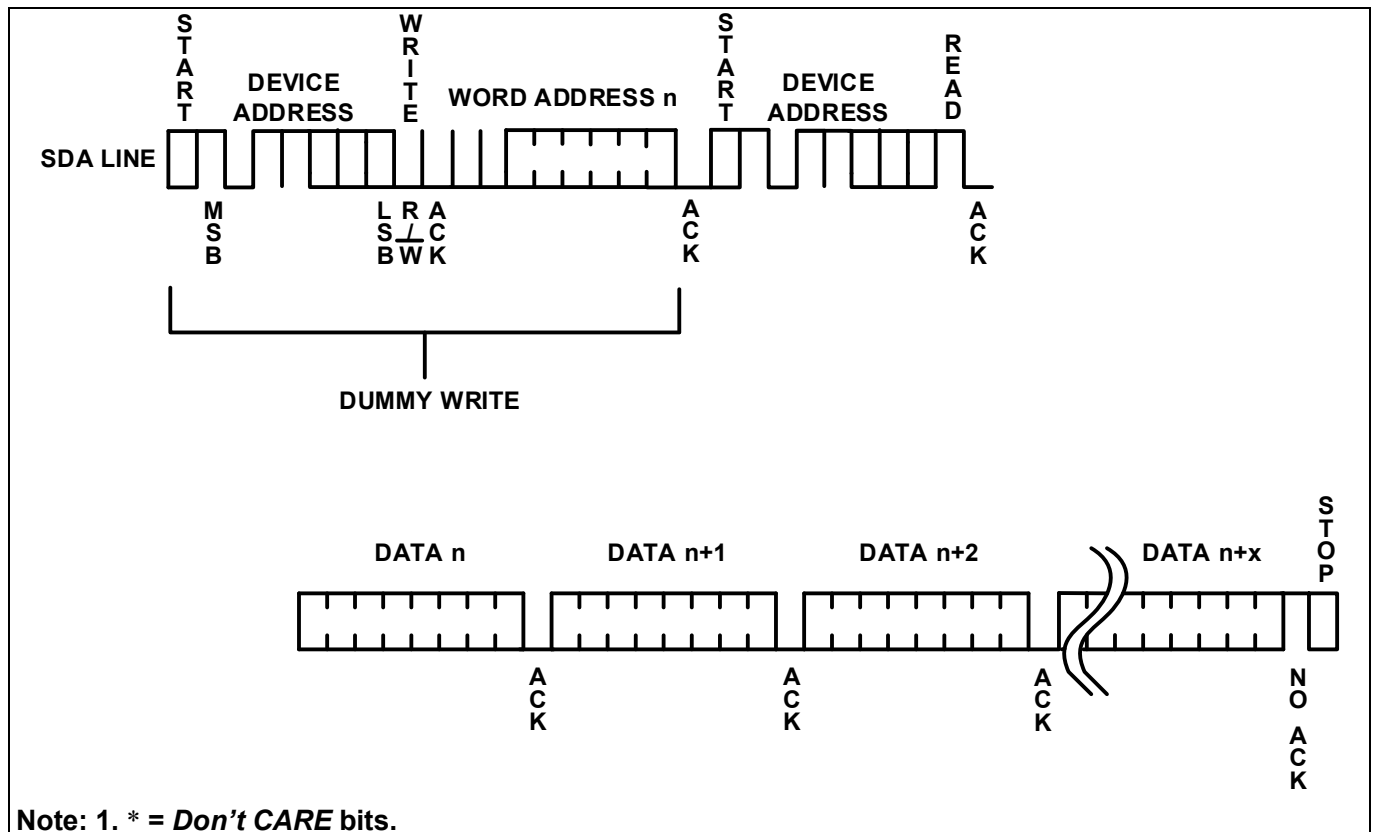


Figure 18. Read Lock Status

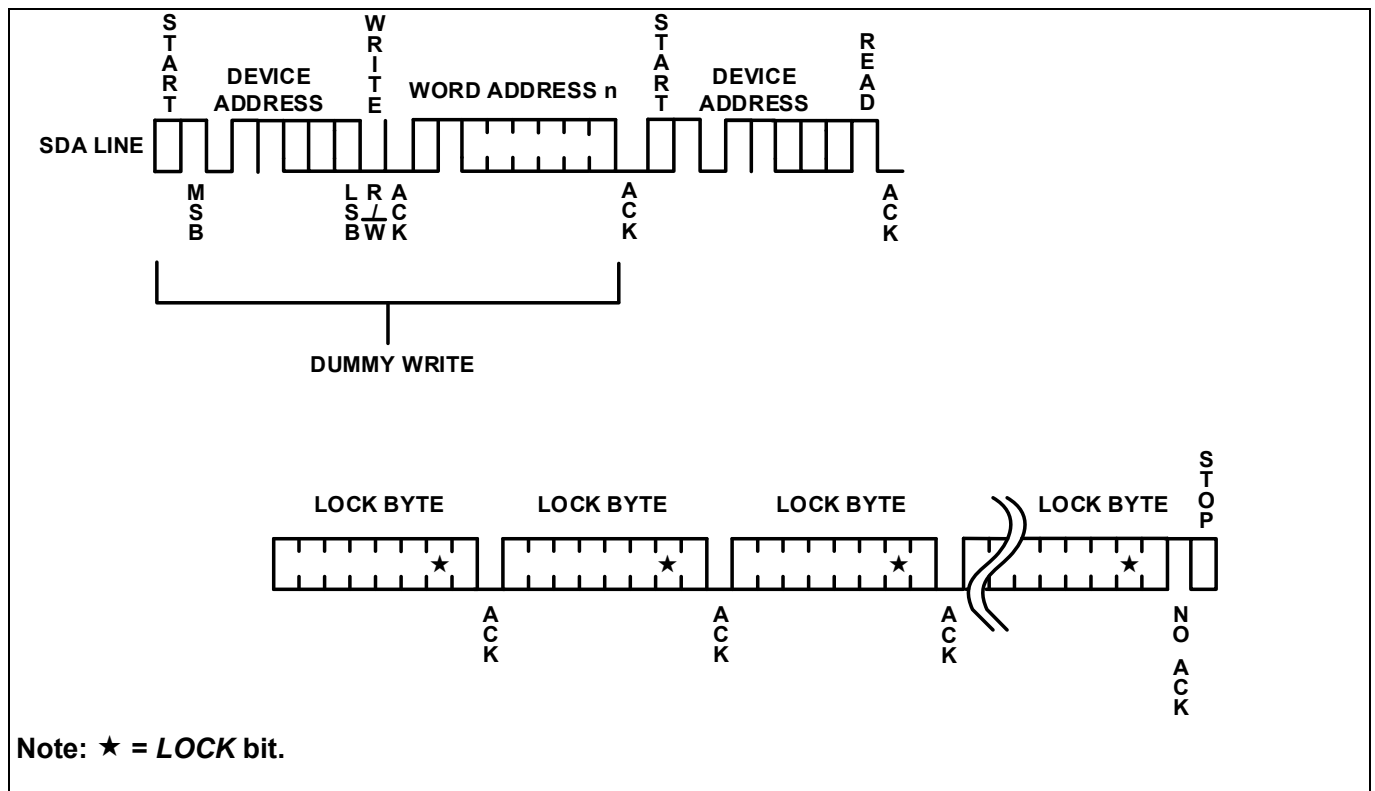


Figure 19. Read Unique ID

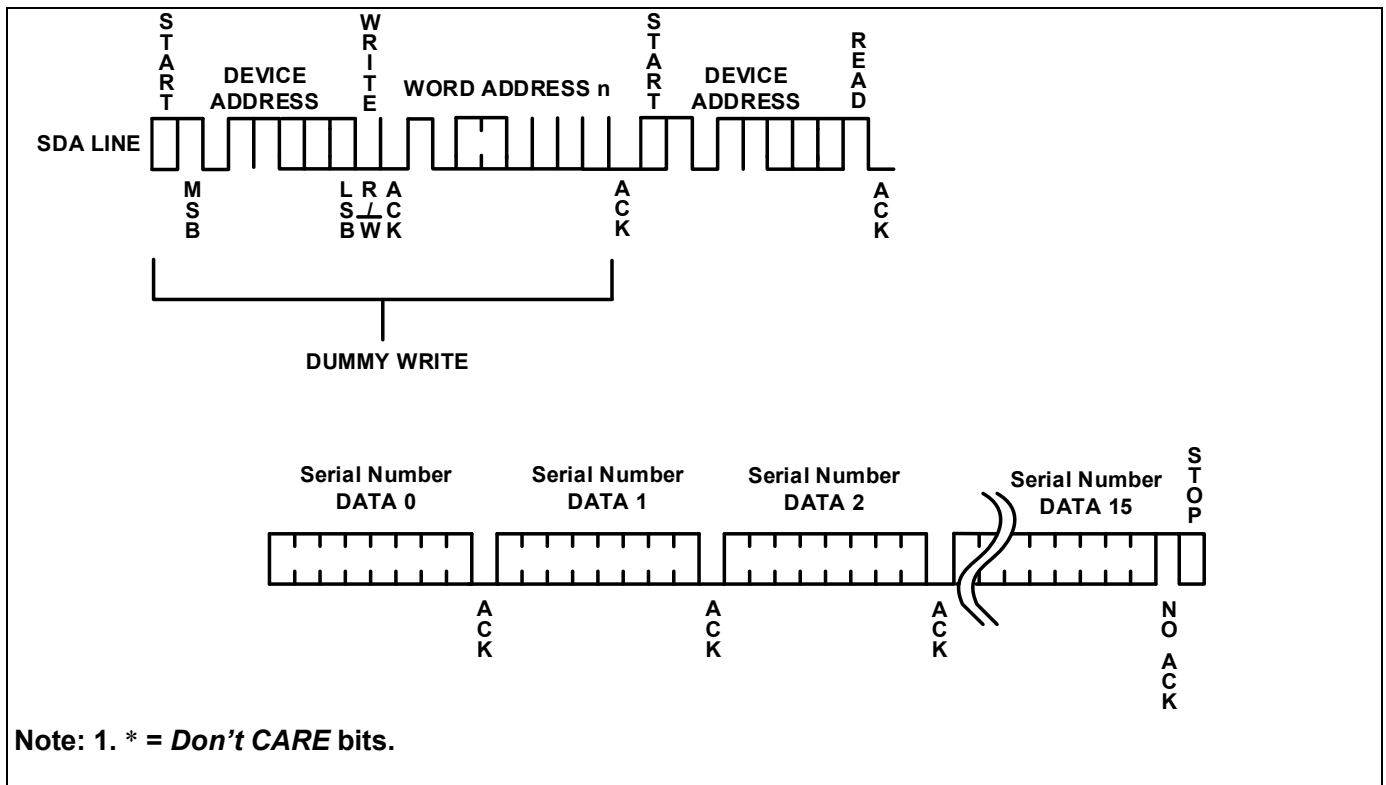


Figure 20. Write SWP

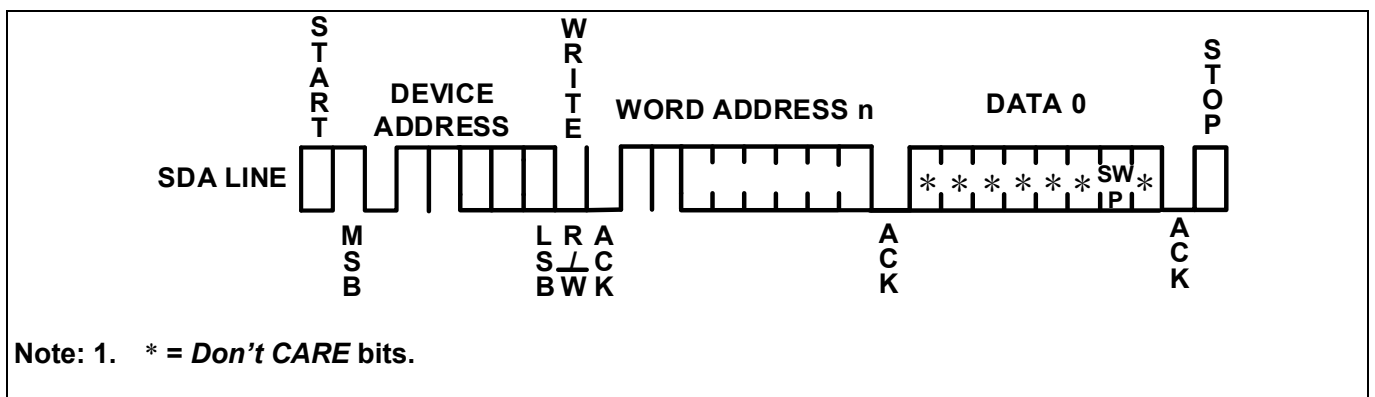
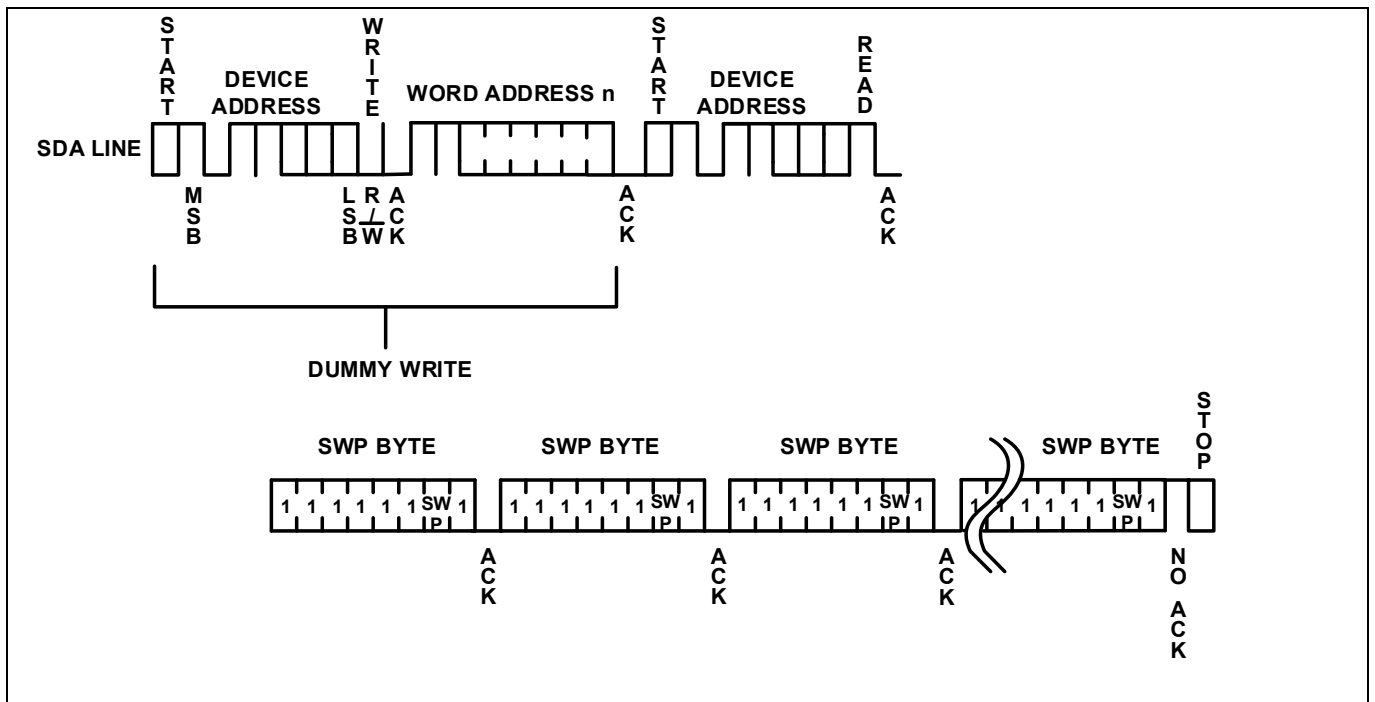


Figure 21. Read SWP





Ordering Information

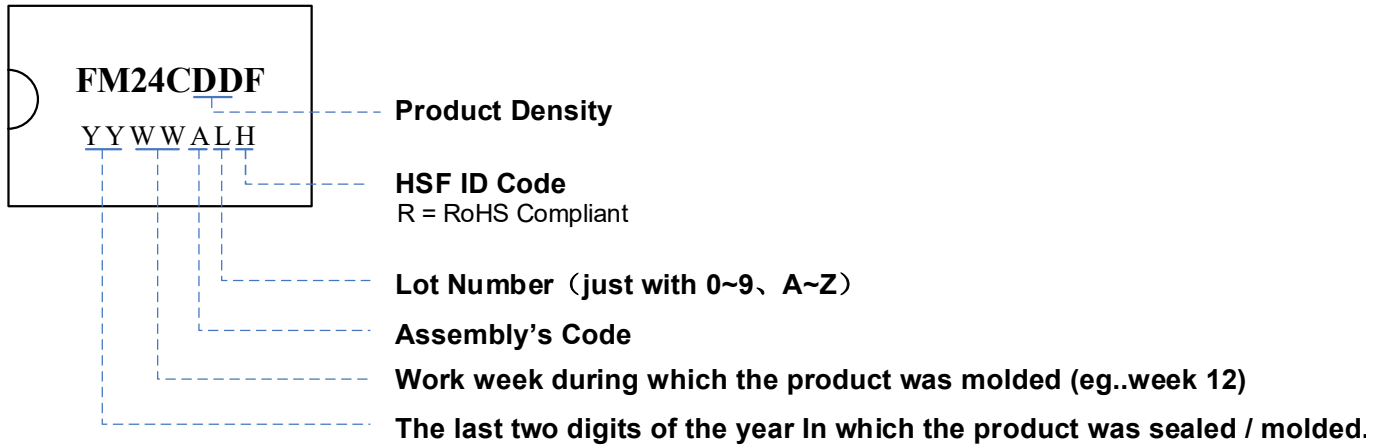
	FM	24C	DD	F	-PP	-C	-H
Company Prefix							
FM = Shanghai Fudan Microelectronics Group Co.,ltd							
Product Family							
24C = 2-Wire Serial EEPROM							
Product Density							
02 = 2K-bit 04 = 4K-bit 08 = 8K-bit							
Device Type							
F = Version							
Package Type							
PD = 8-pin PDIP SO = 8-pin SOP TS = 8-pin TSSOP DN = 8-pin TDFN (2X3mm) ¹ ST = 5-pin TSOT23							
Product Carrier							
U = Tube T = Tape and Reel							
HSF ID Code ²							
R = RoHS Compliant G = RoHS Compliant, Halogen-free, Antimony-free							

Note:

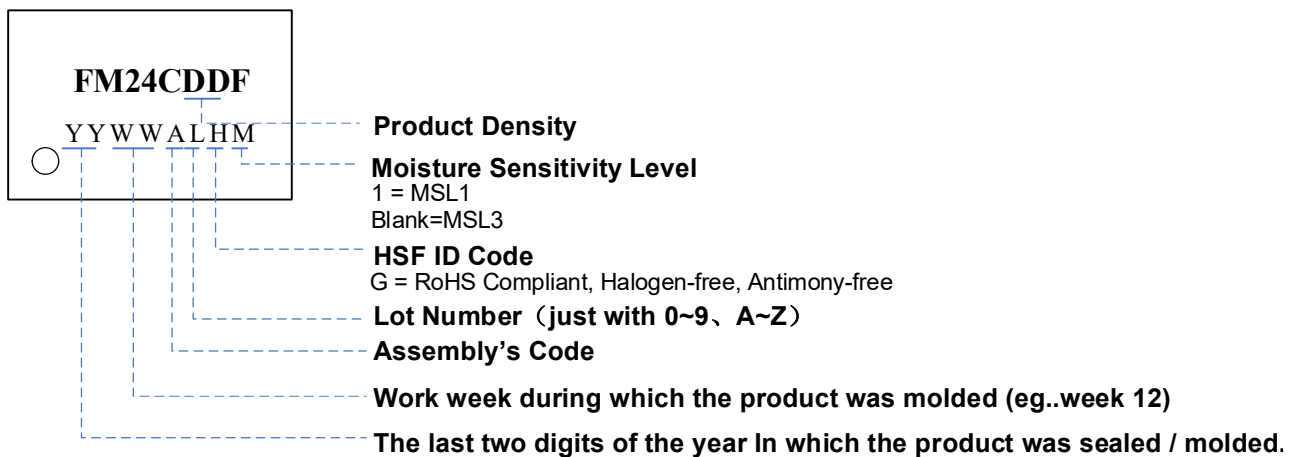
1. For Thinner package please contact local sales office.
2. For PD package: R class only.
For SO, TS, DN and ST package: G class only.

Part Marking Scheme

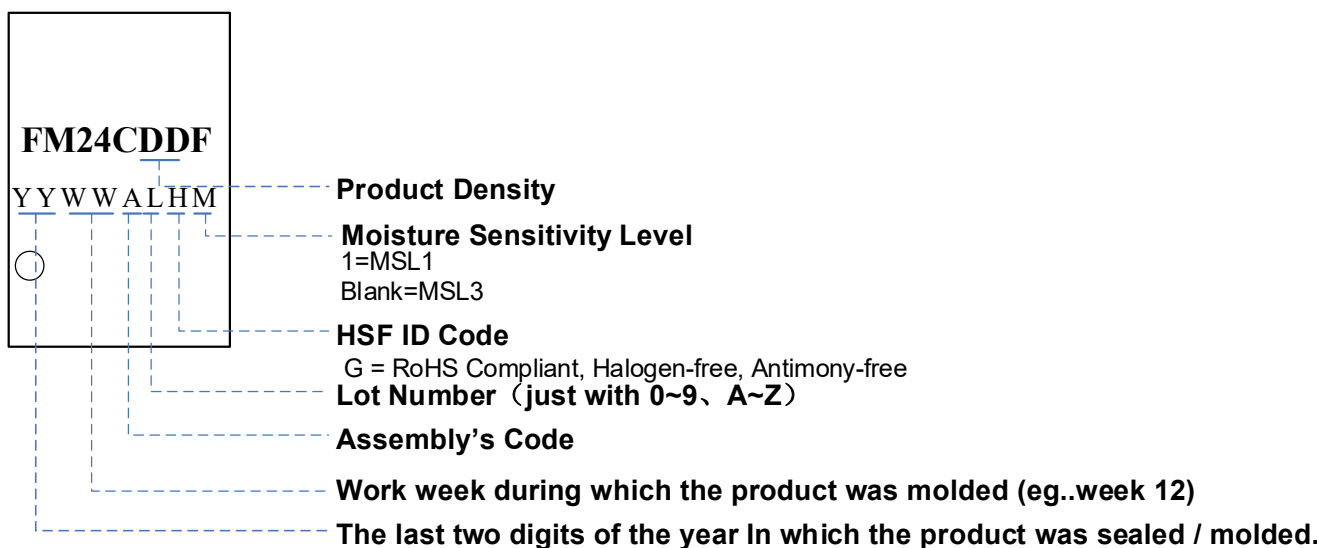
PDIP8

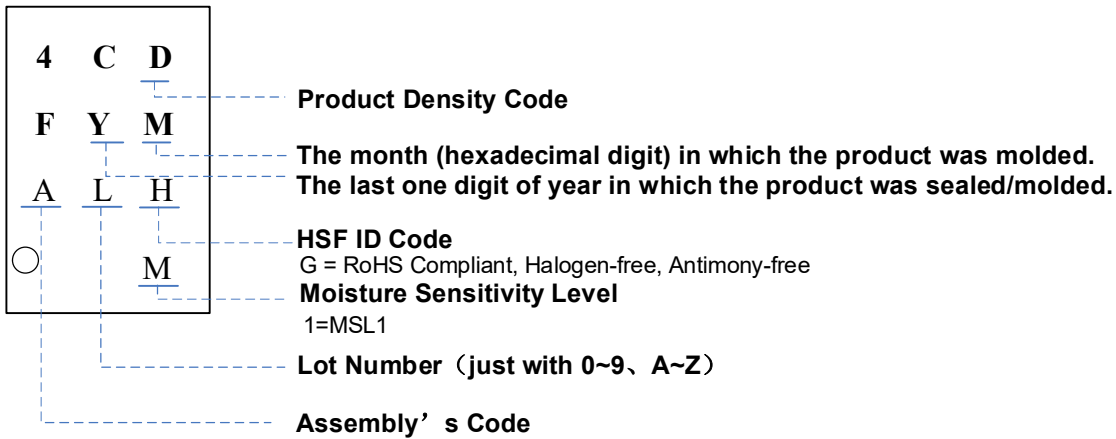
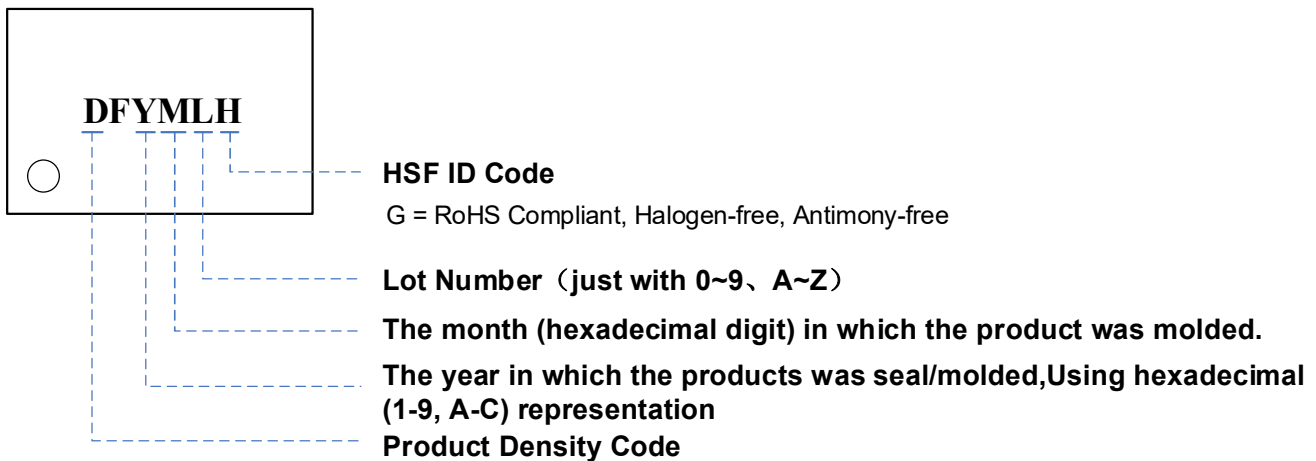


SOP8



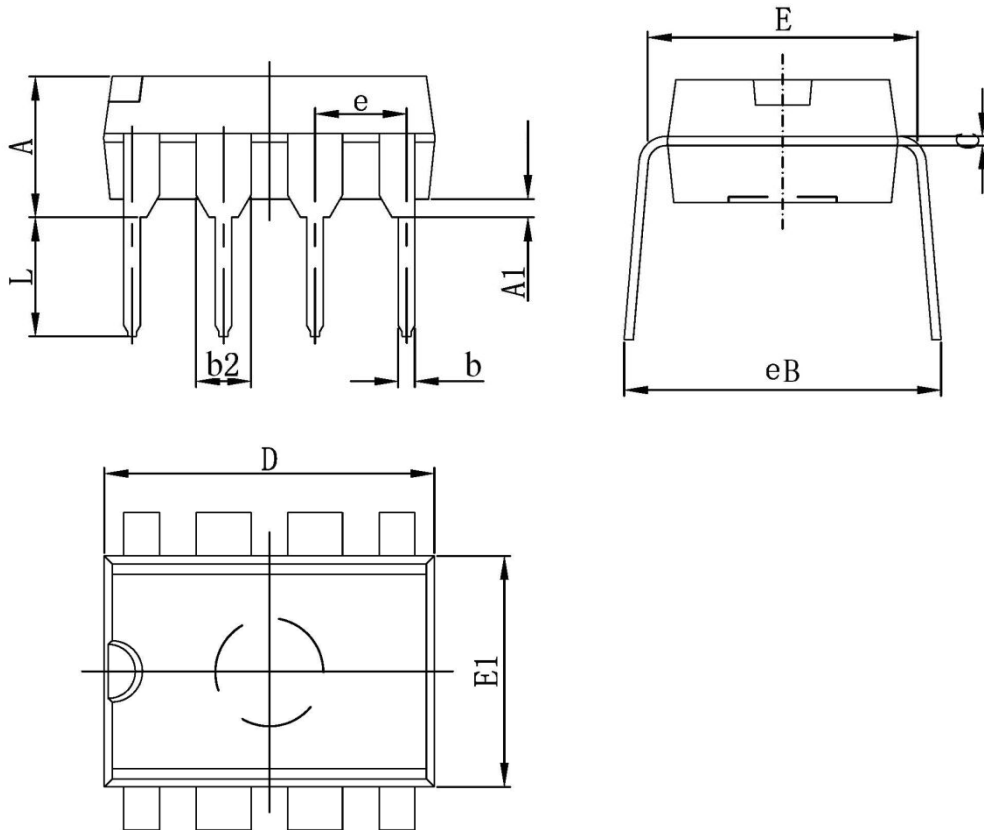
TSSOP8



TDFN8 (2x3mm)**TSOT23-5L**

Packaging Information

PDIP 8

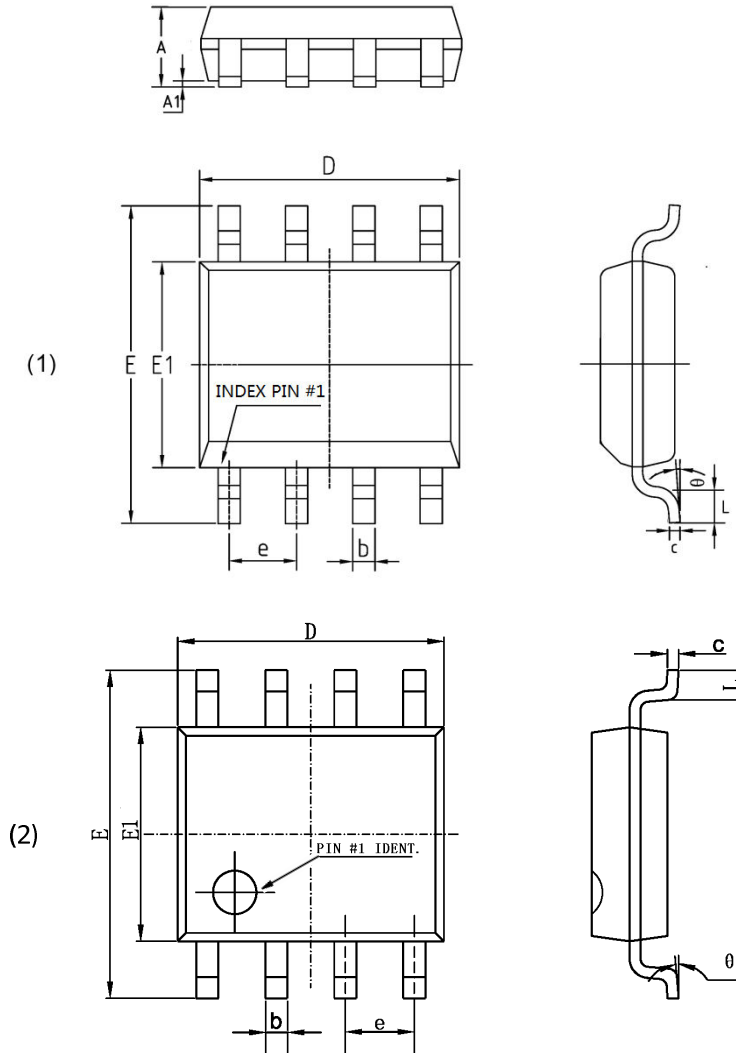


Symbol	MIN	NOM	MAX
A	---	---	5.000
A1	0.380	---	---
b	0.380	0.475	0.570
b2	1.300	1.500	1.700
C	0.200	0.280	0.360
D	9.000	9.500	10.000
E1	6.100	6.550	7.000
E	7.320	7.785	8.250
e	2.540(BSC)		
L	2.920	3.365	3.810
eB	---	---	10.900

NOTE:

1. Dimensions are in Millimeters.

SOP 8

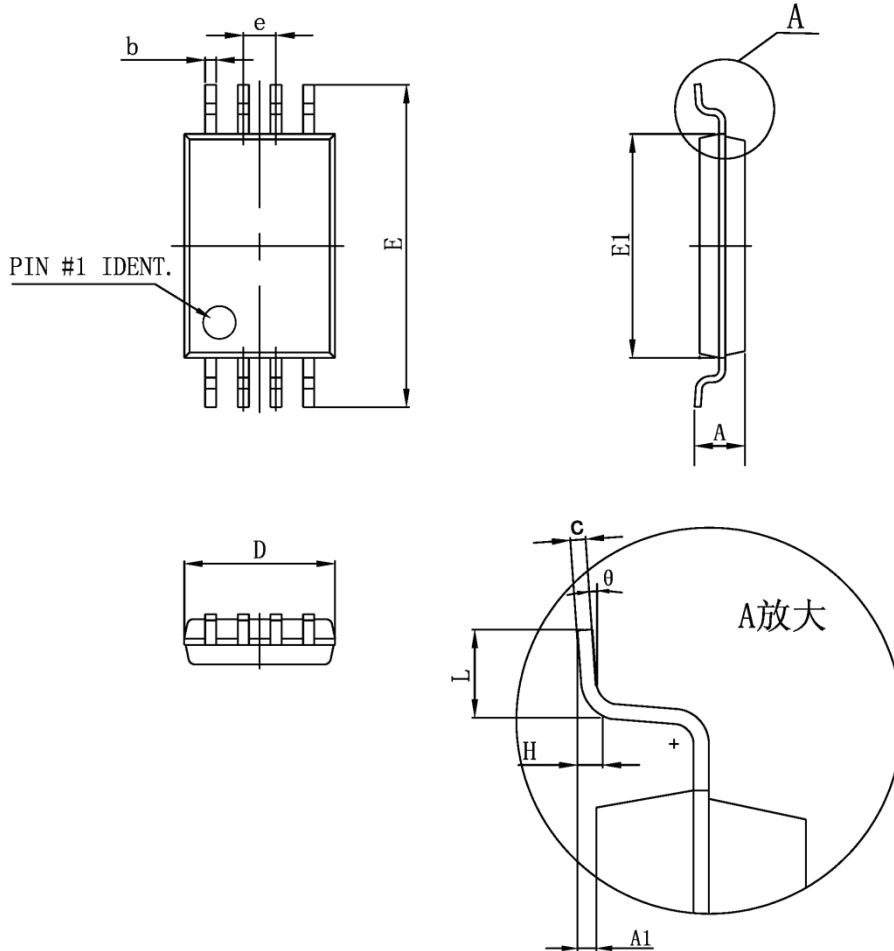


Symbol	MIN	NOM	MAX
A	1.350	1.550	1.750
A1	0.050	0.150	0.250
b	0.330	0.420	0.510
c	0.150	0.200	0.250
D	4.700	4.925	5.150
E1	3.700	3.900	4.100
E	5.800	6.000	6.200
e	1.270(BSC)		
L	0.400	0.650	0.900
θ	0°	4°	8°

NOTE:

1. Dimensions are in Millimeters.

TSSOP8

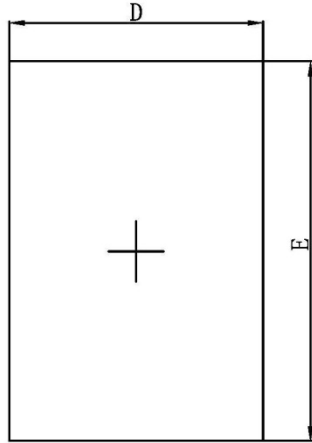


Symbol	MIN	NOM	MAX
D	2.900	3.000	3.100
E1	4.300	4.400	4.500
b	0.190	0.245	0.300
c	0.090	0.145	0.200
E	6.200	6.400	6.600
A	---	---	1.200
A1	0.050	0.100	0.150
e	0.650 (BSC)		
L	0.450	0.600	0.750
θ	0°	4°	8°

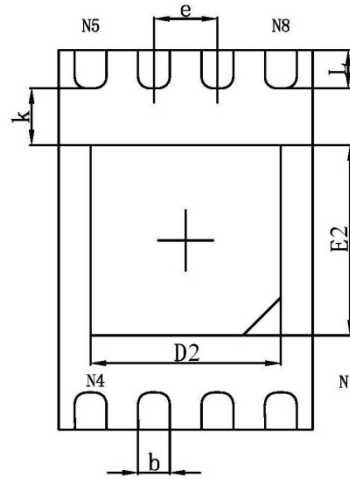
NOTE:

1. Dimensions are in Millimeters.

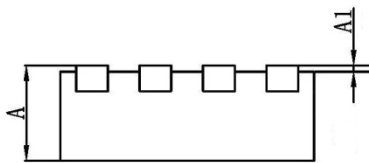
TDFN8(2x3mm)



Top View



Bottom View



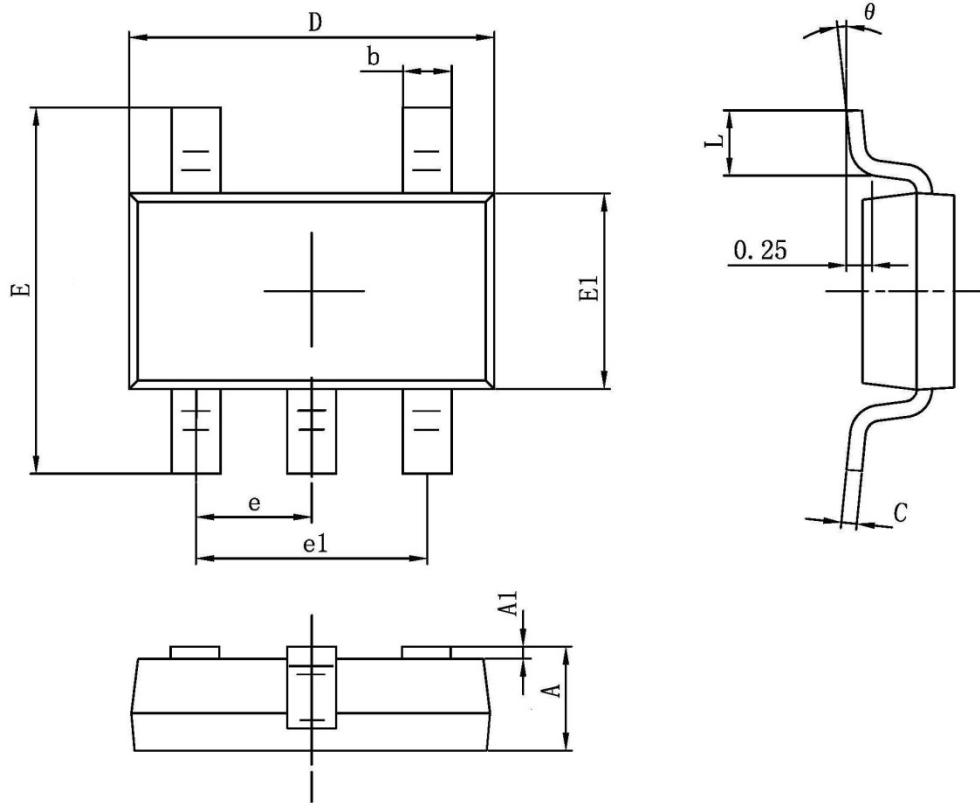
Side View

Symbol	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	0.025	0.050
D	1.900	2.000	2.100
E	2.900	3.000	3.100
D2	1.400	1.500	1.600
E2	1.400	1.550	1.700
k	0.150(MIN)		
b	0.180	0.24	0.300
e	0.500(TYP)		
L	0.200	0.350	0.500

NOTE:

1. Dimensions are in Millimeters.

TSOT23-5L



Symbol	MIN	NOM	MAX
A	0.700	0.800	0.900
A1	0.000	0.050	0.100
b	0.350	0.425	0.500
c	0.080	0.140	0.200
D	2.820	2.920	3.020
E1	1.600	1.650	1.700
E	2.650	2.800	2.950
e	0.950(BSC)		
e1	1.900(BSC)		
L	0.300	0.450	0.600
θ	0°	4°	8°

NOTE:

1. Dimensions are in Millimeters.



Revision History

Version	Publication date	Pages	Revise Description
1.0	Dec. 2020	29	Initial document Release.
1.1	Sep. 2021	30	<ol style="list-style-type: none"> Added Power-up Timing. Updated Packaging Information.
1.2	Sep. 2022	32	<ol style="list-style-type: none"> Added Write Protect Timing. Added t_{WS1}/ t_{WH1}/ t_{WS2}/ t_{WH2} AC parameter. Updated Write Protect description.
1.3	Oct. 2023	31	<ol style="list-style-type: none"> Updated Features. Updated Write Protect Description Updated Device Addressing. Updated DC Characteristics and Power-up Timing parameter. Update Figure 11. Non-Write-Protect Condition. Updated Ordering Information.
1.4	Aug. 2024	32	<ol style="list-style-type: none"> Updated 'Absolute Maximum Ratings'. Updated Write Protect Description Updated Power-up Timing parameter. Updated Packaging Information.



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