Shanghai Fudan Microelectronics Group Company Limited

FM24C32A
2-Wire Serial EEPROM

Data Sheet

Aug. 2018

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Description

The FM24C32A provides 32,768 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 4096 words of 8 bits each. The device's cascadable feature allows up to 8 devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential.
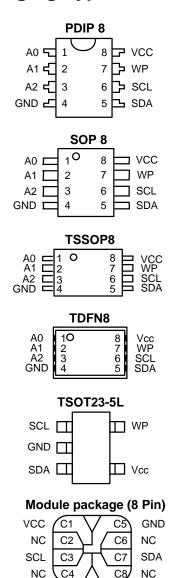
Features

- **Low Operation Voltage: V_{CC} = 1.7V to 5.5V**
- **Internally Organized: 4096 x 8**
- **2-wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bi-directional Data Transfer Protocol**
- **1MHz (2.5V~5.5V) and 400 kHz (1.7V~5.5V) Compatibility**
- **Write Protect Pin for Hardware Data Protection**
- **32-byte Page Write Modes (Partial Page Writes are Allowed)**
- **Self-timed Write Cycle (5 ms max)**
- **High-reliability**
  - **Endurance: 1,000,000 Write Cycles**
  - **Data Retention: 40 Years**
- **PDIP8 Package (RoHS Compliant)**
- **SOP8, TSSOP8, TDFN8 and TSOT23-5L Packages (RoHS Compliant and Halogen-free)**

Absolute Maximum Ratings

Operating Temperature (Plastic Package)	-55 ℃ to +125 ℃
Operating Temperature (Module Package)	-20 ℃ to +60 ℃
Storage Temperature (Plastic Package)	-65 ℃ to +150 ℃
Storage Temperature (Module Package)	-25 ℃ to +70 ℃
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
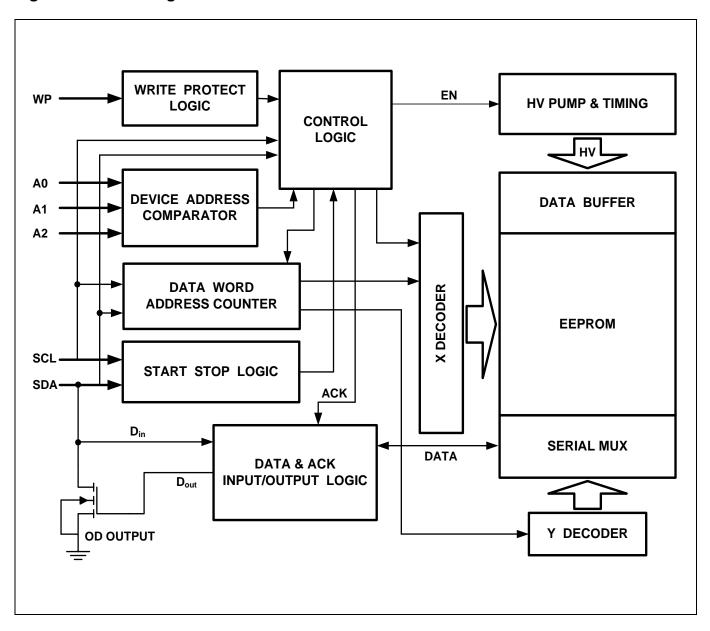
Packaging Type

PDIP 8

A0	1	8	VCC
A1	2	7	WP
A2	3	6	SCL
GND	4	5	SDA

SOP 8

A0	1	8	VCC
A1	2	7	WP
A2	3	6	SCL
GND	4	5	SDA

TSSOP8

A0	1	8	VCC
A1	2	7	WP
A2	3	6	SCL
GND	4	5	SDA

TDFN8

A0	1	8	Vcc
A1	2	7	WP
A2	3	6	SCL
GND	4	5	SDA

TSOT23-5L

SCL	WP
GND	
SDA	Vcc

Module package (8 Pin)

VCC	C1	C5	GND
NC	C2	C6	NC
SCL	C3	C7	SDA
NC	C4	C8	NC

Pin Configurations

Pin Name	Function
A0~A2	Device Address Inputs
SDA	Serial Data Input/Output
SCL	Serial Clock Input
WP	Write Protect
V_{CC}	Power Supply
GND	Ground
NC	Not Connect

Figure 1. Block Diagram

Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hardwired or left not connected for hardware compatibility with other FM24CXX / FM24CXX devices. When the pins are hardwired, as many as eight 32K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). If the pins are left floating, the A2, A1 and A0 pins will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is <3pF, if coupling is >3pF, FMSH recommends connecting the address pins to GND.

WRITE PROTECT (WP): The FM24C32A has a Write Protect pin that provides hardware data protection. The WP pin allows normal write operations when connected to ground (GND). When the Write Protect pin is connected to VCC, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND if the capacitive coupling to the circuit board Vcc plane is <3pF. If coupling is >3pF, FMSH recommends connecting the WP to GND. Switching WP to VCC prior to a write operation creates a software write protected function.

Write Protect Description

WP Pin Status	Part of the Memory Protected
	FM24C32A
WP=V_{CC}	Full (32K) Memory
WP=GND	Normal Read/Write Operations

Memory Organization

FM24C32A, 32K SERIAL EEPROM: Internally organized with 128 pages of 32 bytes each, the 32K requires a 12-bit data word address for random word addressing.

Pin Capacitance

Symbol	Parameter	Test Condition	Max	Units
$C_{IN}^{(1)}$	Input Capacitance	$V_{IN} = 0V$, f = 1MHz	6	pF
$C_{OUT}^{(1)}$	Output Capacitance	$V_{OUT} = 0V$, f = 1MHz	8	pF

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_A = -40 ℃ to +85 ℃, V_{CC} = +1.7V to +5.5V, (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		1.7		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V, Read at 400KHz		0.4	1.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V, Write at 400KHz		2.0	3.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.7V, $V_{IN} = V_{CC}/V_{SS}$			1.0	µA
I_{SB2}	Standby Current	V_{CC} = 5.5V, $V_{IN} = V_{CC}/V_{SS}$			6.0	µA
I_{LI}	Input Leakage Current	$V_{IN} = V_{CC}/V_{SS}$		0.1	3.0	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}/V_{SS}$		0.05	3.0	µA
V_{IL}^{1}	Input Low Level		-0.6		V_{CC} x 0.3	V
V_{IH}^{1}	Input High Level		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level 2	V_{CC} = 3.0V, I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level 1	V_{CC} =1.7V, I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

400KHz

Applicable over recommended operating range from: T_A = -40°C to +85°C, V_{CC} = +1.7V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency, SCL		400	kHz
t_{LOW}	Clock Pulse Width Low	1.3		μs
t_{HIGH}	Clock Pulse Width High	0.6		μs
t_I [1]	Noise Suppression Time		80	ns
t_{AA}	Clock Low to Data Out Valid	0.1	0.9	μs
t_{BUF} [1]	Time the bus must be free before a new transmission can Start	1.3		μs
$t_{HD.STA}$	Start Hold Time	0.6		μs
$t_{SU.STA}$	Start Setup Time	0.6		μs
$t_{HD.DAT}$	Data In Hold Time	0		μs
$t_{SU.DAT}$	Data In Setup Time	100		ns
t_R	Inputs Rise Time [1]		300	ns
t_F	Inputs Fall Time [1]		300	ns
$t_{SU.STO}$	Stop Setup Time	0.6		μs
t_{DH}	Data Out Hold Time	100		ns
t_{WR}	Write Cycle Time		5	ms
Endurance [1]	3.3V, 25°C, Page Mode	1,000,000		Write Cycles

1MHz

Applicable over recommended operating range from: T_A = -40°C to +85°C, V_{CC} = +2.5V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency, SCL		1	MHz
t_{LOW}	Clock Pulse Width Low	500		ns
t_{HIGH}	Clock Pulse Width High	320		ns
t_I [1]	Noise Suppression Time		80	ns
t_{AA}	Clock Low to Data Out Valid		450	ns
t_{BUF} [1]	Time the bus must be free before a new transmission can Start	500		ns
$t_{HD.STA}$	Start Hold Time	250		ns
$t_{SU.STA}$	Start Setup Time	250		ns
$t_{HD.DAT}$	Data In Hold Time	0		ns
$t_{SU.DAT}$	Data In Setup Time	50		ns
t_R	Inputs Rise Time [1]		120	ns
t_F	Inputs Fall Time [1]		120	ns
$t_{SU.STO}$	Stop Setup Time	250		ns
t_{DH}	Data Out Hold Time	100		ns
t_{WR}	Write Cycle Time		5	ms

Symbol	Parameter	Min	Max	Units
Endurance [1]	3.3V, 25 ℃, Page Mode	1,000,000		Write Cycles

Notes: 1. This parameter is characterized and is not 100% tested.

      2. AC measurement conditions:

         RL (connects to V_{CC}): 1.3 kΩ

         Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}

         Input rise and fall times: ≤ 50 ns

         Input and output timing reference voltages: 0.5 V_{CC}

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Figure 4). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Figure 5).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Figure 5).

ACKNOWLEDGE: All address and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

STANDBY MODE: The FM24C32A features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the stop bit and the completion of any internal operations.

Memory RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset in following these steps:

1. Clock up to 9 Cycles,
2. Look for SDA high in each cycle while SCL is high and then,
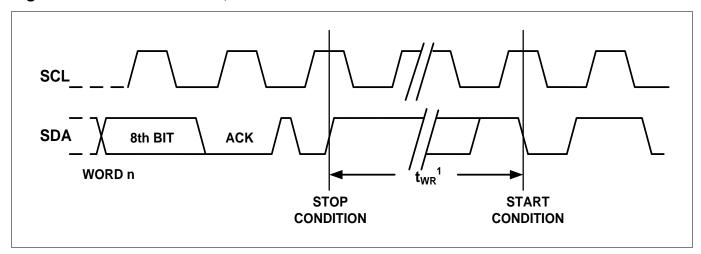3. Create a start condition as SDA is high.

Bus Timing

Figure 2. SCL: Serial Clock, SDA: Serial Data I/O

Write Cycle Timing

Figure 3. SCL: Serial Clock, SDA: Serial Data I/O

Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.
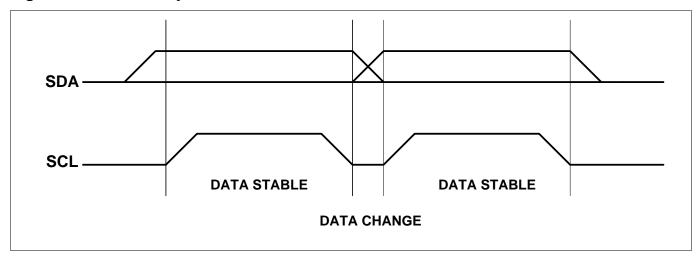
Figure 4. Data Validity
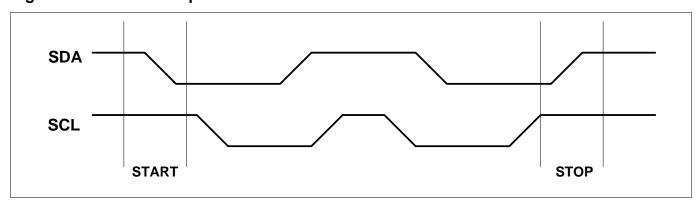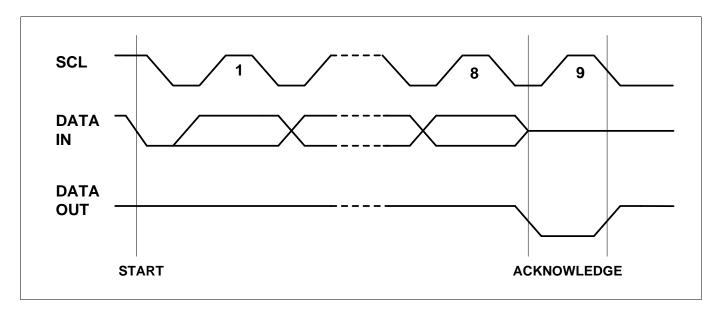

Figure 5. Start and Stop Definition

Figure 6．Output Acknowledge

Device Addressing

The 32K EEPROM device requires a 8-bit device address word following a start condition to enable the chip for a read or write operation (refer to Figure 7).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown. This is common to all the EEPROM devices.

The 32K EEPROM uses the three device address bits A2, A1, A0 to allow as many as eight devices on the same bus. These bits must compare to their corresponding hard-wired input pins. The A2, A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The Module package device address word also consists of a mandatory one, zero sequence for the first four most significant bits. The next 3 bits are all zero.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to a standby state.

NOISE PROTECTION: Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device.

DATA SECURITY: The FM24C32A has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at V_{CC}.

Write Operations

BYTE WRITE: A write operation requires two 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (refer to Figure 8).

PAGE WRITE: The 32K EEPROM is capable of 32-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Figure 9).

The data word address lower five bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (refer to Figure 10).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 11).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero but does generate a following stop condition (refer to Figure 12).
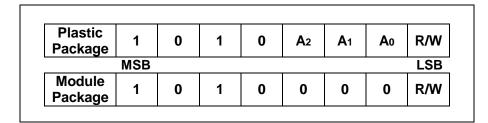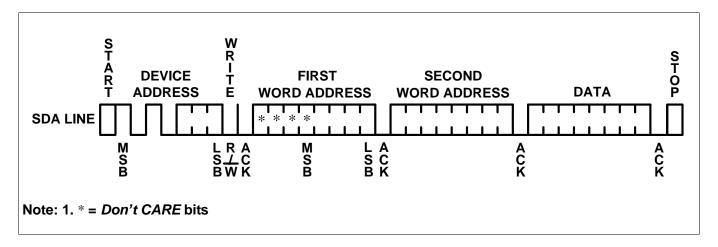
Figure 7. Device Address

Plastic Package	1	0	1	0	A$_2$	A$_1$	A$_0$	R/W
MSB								LSB
Module Package	1	0	1	0	0	0	0	R/W

Figure 8. Byte Write

Note: 1. ∗ = *Don't CARE* bits
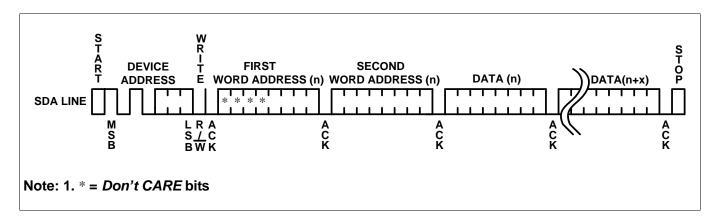
Figure 9. Page Write

Note: 1. ∗ = *Don't CARE* bits

Figure 10. Current Address Read

Figure 11. Random Read

Note: 1. ∗ = Don't CARE bits.

Figure 12. Sequential Read

Ordering Information

```
                              FM   24C   32   A  -PP  -C  -H
```

Company Prefix

FM = Shanghai Fudan Microelectronics Group Co.,ltd

Product Family

24C = 2-Wire Serial EEPROM

Product Density

32 = 32K-bit

Supply Voltage

A = 1.7V to 5.5V

Package Type

PD = 8-pin PDIP   M2F or M2P = 8-pin Module Package [1]
SO = 8-pin SOP
TS = 8-pin TSSOP
DN = 8-pin TDFN
ST = 5-pin TSOT23

Product Carrier

U = Tube
T = Tape and Reel
R = Module Reel

HSF ID Code [2]

Blank or R = RoHS Compliant
G = RoHS Compliant, Halogen-free, Antimony-free

Note: 1. For the details of Module package and MSL1 package please contact local sales office.
      2. For the TDFN8 and TSOT23-5L, only offers the package compliant with G-class.
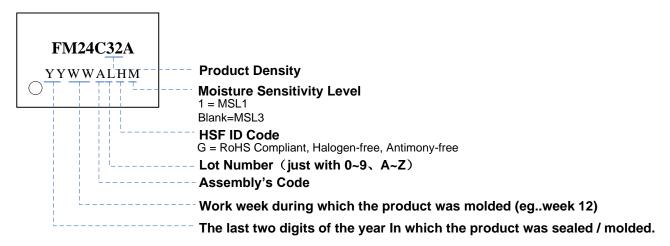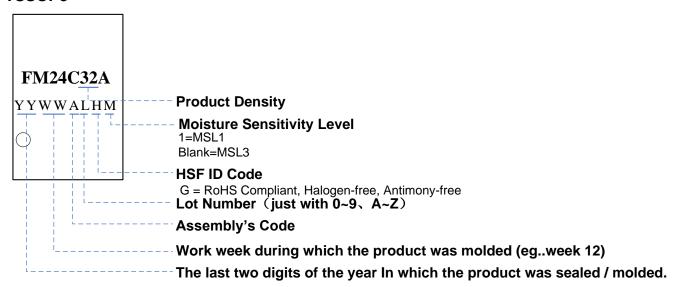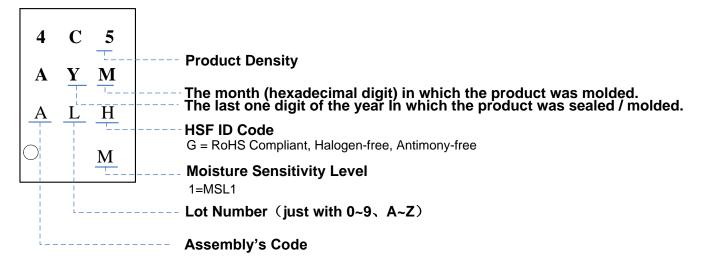
Part Marking Scheme

PDIP8
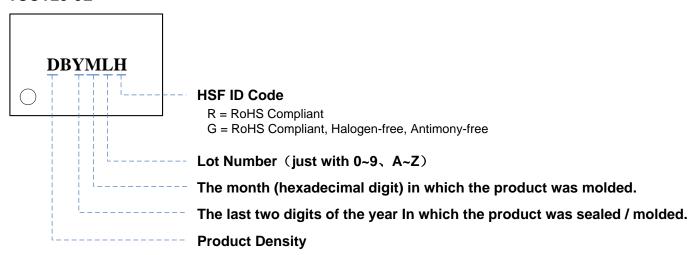
FM24C32A

YYWWALH

- - - - **Product Density**

- - - - **HSF ID Code**
   R = RoHS Compliant
   G = RoHS Compliant, Halogen-free, Antimony-free

- - - - **Lot Number**（just with **0~9、A~Z**）

- - - - **Assembly's Code**

- - - - **Work week during which the product was molded (eg..week 12)**

- - - - **The last two digits of the year In which the product was sealed / molded.**

SOP8

FM24C32A

YYWWALHM

- - - - **Product Density**

- - - - **Moisture Sensitivity Level**
   1 = MSL1
   Blank=MSL3

- - - - **HSF ID Code**
   G = RoHS Compliant, Halogen-free, Antimony-free

- - - - **Lot Number**（just with **0~9、A~Z**）

- - - - **Assembly's Code**

- - - - **Work week during which the product was molded (eg..week 12)**

- - - - **The last two digits of the year In which the product was sealed / molded.**

TSSOP8

FM24C32A

YYWWALHM

- - - - **Product Density**

- - - - **Moisture Sensitivity Level**
   1=MSL1
   Blank=MSL3

- - - - **HSF ID Code**
   G = RoHS Compliant, Halogen-free, Antimony-free

- - - - **Lot Number**（just with **0~9、A~Z**）

- - - - **Assembly's Code**

- - - - **Work week during which the product was molded (eg..week 12)**

- - - - **The last two digits of the year In which the product was sealed / molded.**

TDFN8

```
4  C  5
A  Y  M
A  L  H
○     M
```

Product Density

The month (hexadecimal digit) in which the product was molded.
The last one digit of the year In which the product was sealed / molded.

HSF ID Code
G = RoHS Compliant, Halogen-free, Antimony-free

Moisture Sensitivity Level
1=MSL1

Lot Number（just with 0~9、A~Z）

Assembly's Code

TSOT23-5L

```
   DBYMLH
○
```

HSF ID Code
R = RoHS Compliant
G = RoHS Compliant, Halogen-free, Antimony-free

Lot Number（just with 0~9、A~Z）

The month (hexadecimal digit) in which the product was molded.

The last two digits of the year In which the product was sealed / molded.

Product Density

Packaging Information

PDIP 8

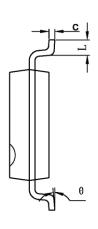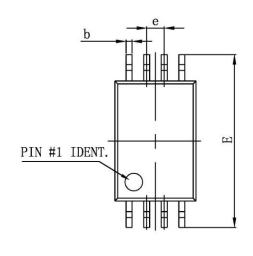| Symbol	MIN	MAX
A	---	5.000
A1	0.380	---
b	0.380	0.570
b2	1.300	1.700
C	0.200	0.360
D	9.000	10.000
E1	6.100	7.000
E	7.320	8.250
e	2.540(BSC)	
L	2.920	3.810
eB	---	10.900

NOTE:
1. Dimensions are in Millimeters.

SOP 8

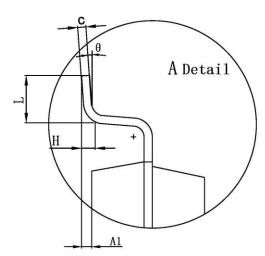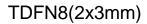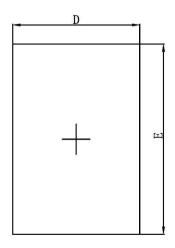| Symbol	MIN	MAX
A	1.350	1.750
A1	0.050	0.250
b	0.330	0.510
c	0.150	0.260
D	4.700	5.150
E1	3.700	4.100
E	5.800	6.200
e	1.270(BSC)	
L	0.400	1.270
θ	0°	8°

NOTE:
1. **Dimensions are in Millimeters.**

TSSOP8

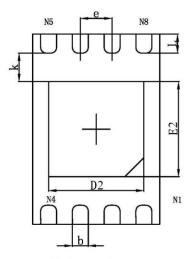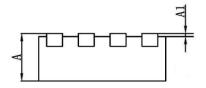| Symbol	MIN	MAX
D	2.900	3.100
E1	4.300	4.500
b	0.190	0.300
c	0.090	0.200
E	6.200	6.600
A		1.200
A1	0.050	0.150
e	0.650 (BSC)	
L	0.450	0.750
θ	0°	8°

NOTE:
1. **Dimensions are in Millimeters.**

TDFN8(2x3mm)

Top View

Bottom View

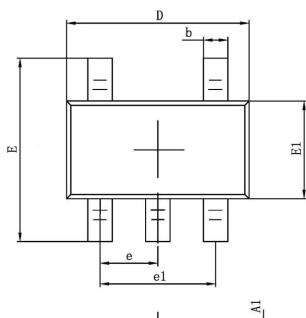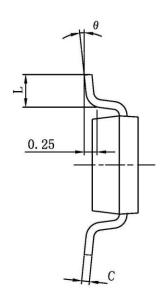**Side View**

Symbol	MIN	MAX
A	0.700	0.80
A1	0.000	0.050
D	1.900	2.100
E	2.900	3.100
D2	1.400	1.600
E2	1.400	1.700
k	0.150(MIN)	
b	0.200	0.300
e	0.500(TYP)	
L	0.200	0.500

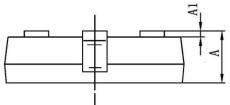NOTE:
1. Dimensions are in Millimeters.

TSOT23-5L

Symbol	MIN	MAX
A	0.700	0.900
A1	0.000	0.100
A2	0.700	0.800
b	0.350	0.500
c	0.080	0.200
D	2.820	3.020
E1	1.600	1.700
E	2.650	2.950
e	0.950(BSC)	
e1	1.900(BSC)	
L	0.300	0.600
θ	0°	8°

NOTE:
1. Dimensions are in Millimeters.

Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
1.0	May 2011	22		Initial document Release.
2.0	Jan 2013	23	"Feature" "Package type" "DC Characteristics" "AC Characteristics" "Packaging Information" "Disclaimer" "Ordering Information" "Part Marking Scheme"	1. Updated the "Features", changed the data retention spec to 40 years. 2. Updated the "Packaging Type", deleted the 6PIN module package. 3. Updated the "DC Characteristics". 4. Updated the "AC Characteristics". 5. Updated the package information of PDIP8, TSSOP8 and TDFN8. 6. Updated the "Disclaimer". 7. Updated the "Ordering Information". 8. Updated the "Part Marking Scheme".
2.1	Apr. 2013	24	"Package type" "Ordering Information" "Packaging Information" "Sales and Service"	1. Added TSOT23-5L Package offering. 2. Updated the "Sales and Service"
2.2	Aug. 2018	24	Packaging Information	Updated the "Packaging Information".

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