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FM25NQ04T1/T2/T3/T4
NFC Serial Flash

Data Sheet

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1 Description

FM25NQ04Tx is a 4Mbit dual interface Flash with flexible tag function. The 4Mbit data memory and the dedicated tag memory can be accessed by both SPI interface and ISO/IEC 14443A compatible RF interface. When tag memory accessed by RF interface, the device is fully compatible with NFC Forum Type 2 tag. The device can also access tag memory through the conventional address by SPI interface. This feature ensures a flexible NFC tag application.

2 Features

- **Contact Interface**
  - 2.7V~3.6V single power supply
  - Typical standby current <5uA
  - Standard SPI: CLK, CS#, DI, DO, WP#
  - Dual SPI: CLK, CS#, DQ0, DQ1, WP#
  - Quad SPI: CLK, CS#, DQ0, DQ1, DQ2, DQ3
  - QPI: CLK, CS#, DQ0, DQ1, DQ2, DQ3
  - Max data memory FAST_READ clock frequency: 50MHz
  - Max data memory READ clock frequency: 33MHz
  - Typical data memory page program time: 0.35ms
  - Typical data memory sector erase time: 50ms
  - Typical data memory block erase time: 500ms
  - Typical data memory chip erase time: 32s
  - Byte and Page Write (up to 16 bytes) for tag memory
  - Random and Sequential read for tag memory
  - 5MHz compatibility for tag memory operation

- **RF Interface**
  - ISO/IEC 14443A compatible
  - Contactless data transmission
  - Enhanced RF performance using contact power
  - Carrier frequency: 13.56 MHz
  - Data transfer rate: 106/212/424/848 kbit/s
  - UID & Counter ASCII Mirror for automatic serialization NDEF messages
  - Originality signature
  - True anticollision
  - Tag operation: 4 bytes Write, 16 bytes /Fast Read
  - Data Memory operation: Page program (up to 256 bytes), sector/block erase, Random read (up to 256 bytes)
  - Support sleep mode

- **Memory**
  - Data Memory: 4Mbit Flash
    128 uniform sectors with 4K-byte each
    8 uniform blocks with 64K-byte each or
    16 uniform blocks with 32K-byte each
    256 bytes per programmable page
    100,000 program/erase cycles
    Data retention: 20 years
  - Tag Memory:

Part number	Tag memory - user data
FM25NQ04T1	144 bytes
FM25NQ04T2	504 bytes
FM25NQ04T3	888 bytes
FM25NQ04T4	1884 bytes

    Self-timed write cycle (5 ms max)
    Endurance: 1 million write cycles
    Data retention: 40 years

- **Security**
  - Software and hardware write protection for data memory
  - Software write protection of tag memory in SPI interface
  - Password protection for status register and RF data write
  - Unique ID for each device

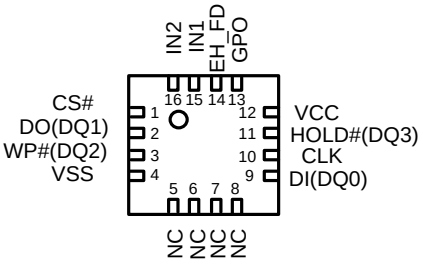
- **User configurable General purpose output**

- **Energy harvesting and Field detection**
  - Configurable Energy harvesting(EH) or Field detection(FD) output
  - Configurable EH output voltage: 1.5V, 1.8V，2.5V and 3.3V
  - Configurable EH limited current:: 0.5mA, 1mA, 2mA and no limit
  - Configurable FD output voltage: 1.5V, 1.8V，2.5V and 3.3V
  - Configurable FD trigger action: upon any RF field presence, upon request, upon the selection of the tag and upon halt with previous read operation

- **Green Package**
  - RoHS Compliant and Halogen-free

3 Packaging Type

QFN16



4 Pin Configurations

Pin Name	Function
EH_FD	Energy harvesting and Field Detection Output
GPO	General purpose output
IN1/IN2	Antenna connection
VCC	Power Supply
VSS	Ground
CS#	Chip Select Input
DO (DQ_1)	Data Output (Data Input Output 1)(1)
WP# (DQ_2)	Write Protect Input (Data Input Output 2)(2)
DI (DQ_0)	Data Input (Data Input Output 0)(1)
CLK	Serial Clock Input
HOLD# (DQ_3)	Hold Input (Data Input Output 3)(2)

5 Block Diagram

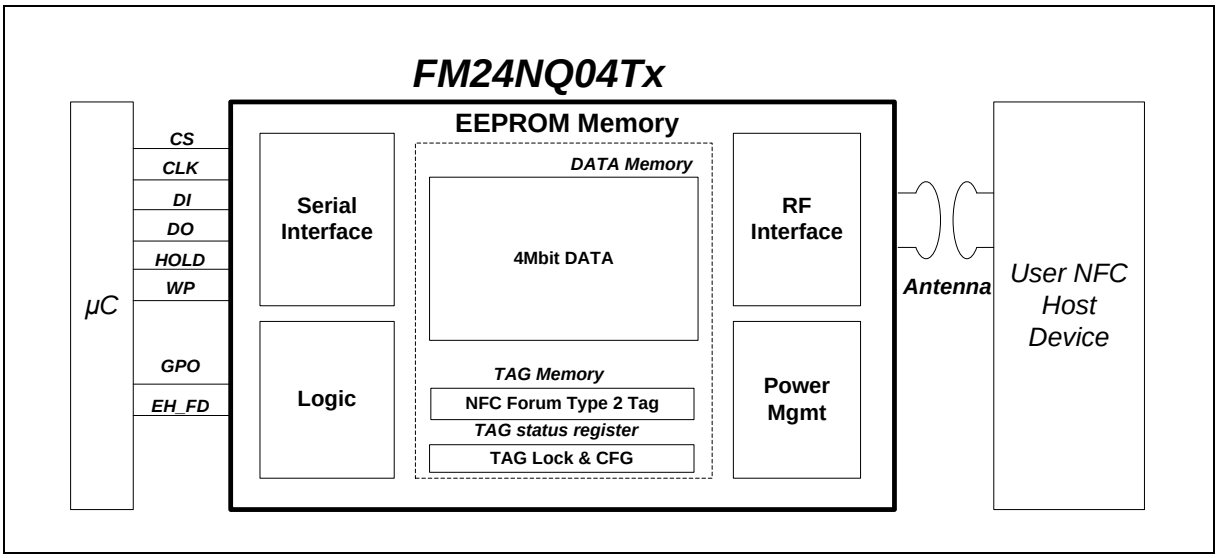


Figure 1 Block Diagram of FM25NQ04Tx

6 Pin Descriptions

6.1 SPI interface PIN

Serial Clock (CLK): The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.

Serial Data Input, Output and I/Os (DI, DO and DQ_0, DQ_1, DQ_2, DQ_3): The FM25NQ04TX supports standard SPI, Dual SPI, Quad SPI and QPI operation. Standard SPI commands use the unidirectional DI (input) pin to serially write commands, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual/Quad SPI and QPI commands use the bidirectional DQ pins to serially write commands, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI and QPI commands require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the WP# pin becomes DQ_2 and HOLD# pin becomes DQ_3.

Chip Select (CS#): The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high, the device is deselected and the Serial Data Output (DO, or DQ_0, DQ_1, DQ_2, DQ_3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When CS# is brought low, the device will be selected, power consumption will increase to active levels and commands can be written to and data read from the device. After power-up, CS# must transition from high to low before a new command will be accepted. The CS# input must track the VCC supply level at power-up (see “7.1.1 Data memory write protection” and “Figure 118 Power-up Timing”). If needed a pull-up resister on CS# can be used to accomplish this.

HOLD (HOLD#): The HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don’t care). When HOLD**#** is brought high, device operation can resume. The HOLD# function can be useful when multiple devices are sharing the same SPI signals. The HOLD# pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the HOLD# pin function is not available since this pin is used for DQ_3.

Write Protect (WP#): The Write Protect (WP#) pin can be used to prevent the Status Registers from being written. Used in conjunction with the Status Register’s Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The WP# pin is active low. However, when the QE bit of Status Register-2 is set for Quad I/O, the WP# pin function is not available since this pin is used for DQ_2.

6.2 Antenna Connection (IN1, IN2)

These input pins are used to connect the device to an external coil exclusively. It is advised to not connect any other DC or AC path to IN1 and IN2 pads. When correctly tuned, the coil is used to access the device using the ISO/IEC 14443A protocol and NFC Forum Type 2 Tag Operation Specification.

6.3 Energy Harvesting and Field Detection Output (EH_FD)

This output pin is used to deliver the analog voltage available when the RF field strength is sufficient. The output voltage and the drive current can be configured.

This pin is also used as RF field detection and to interrupt source to e.g. wake up an embedded microcontroller or trigger further actions. Typical applications are Bluetooth and Wi-Fi pairing.

6.4 General purpose Output (GPO)

This configurable output signal is used either to indicate that the FM25NQ04Tx is executing an internal write cycle of data or tag memory via RF interface or than an RF command is in progress. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from GPO to system power.

6.5 Ground (VSS)

VSS is the reference for the VCC supply voltage.

6.6 Supply voltage (VCC)

This pin can be connected to an external DC supply voltage not only in SPI interface, but also in RF interface.

Prior to selecting the memory and issuing command to it, a valid and stable VCC voltage within the specified [VCC(min), VCC(max)] range must be applied. To maintain a stable DC supply voltage, it is recommended to decouple the VCC line with a suitable capacitor (usually of the order of 10 nF) close to the VCC/VSS package pins. This voltage must remain stable and valid until the end of the transmission of the command and, for a write command, until the completion of the internal write cycle (t_{WR}).

7 Memory Organization

The FM25NQ04Tx memory consists of two parts: Data memory and Tag memory. Each part can be accessed by SPI interface or RF interface.

Table 1 Memory organization of FM25NQ04Tx.

Data memory organization

Contact interface	RF interface	Block address (64KB)	Block address (32KB)	Sector address (4KB)	Byte Address Range		Description
SPI data command	RF data command	7	15 | 14	127	07F000h	07FFFFh	Data memory 4Mbit
				…	…	…	
				112	070000h	070FFFh	
		6	13 | 12	111	06F000h	06FFFFh	
				…	…	…	
				96	060000h	060FFFh	
		5	11 | 10	95	05F000h	05FFFFh	
				…	…	…	
				80	050000h	050FFFh	
		4	9 | 8	79	04F000h	04FFFFh	
				…	…	…	
				64	040000h	040FFFh	
		3	7 | 6	63	03F000h	03FFFFh	
				…	…	…	
				48	030000h	030FFFh	
		2	5 | 4	47	02F000h	02FFFFh	
				…	…	…	
				32	020000h	020FFFh	
		1	3 | 2	31	01F000h	01FFFFh	
				…	…	…	
				16	010000h	010FFFh	
		0	1 | 0	15	00F000h	00FFFFh	
				…	…	…	
				2	002000h	002FFFh	
				1	001000h	001FFFh	
				0	000000h	000FFFh	

TAG memory organization

Contact Interface	RF Interface	Address		Byte number inside page			Description
		Page	Byte	0	…	15	
SPI tag command	TAG memory command	000h	0000h	TAG memory (12 page X 16 byte for FM25NQ04T1 34 page X 16 byte for FM25NQ04T2 58 page X 16 byte for FM25NQ04T3 120 page X 16 byte for FM25NQ04T4)			TAG memory
		001h	0010h				
		…	…				
		077h	0770h				

Remark: The address not mentioned is NULL, which indicates the empty address. When accessed by contact interface, the readout data is always 00h.

7.1 Data memory

The data memory of FM25NQ04Tx is organized into 2,048 programmable pages of 256-bytes each which can be accessed by SPI interface or RF interface, using 3 bytes address. Up to 256 bytes can be programmed (bits are programmed from 1 to 0) at a time. Pages can be erased in groups of 16 (4KB sector erase), groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The FM25NQ04Tx has 128 erasable sectors, 16 erasable 32-k byte blocks and 8 erasable 64-k byte blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage.

7.1.1 Data memory write protection

7.1.1.1 Data memory write protection in SPI interface

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern, the FM25NQ04TX provides several means to protect the data from inadvertent writes by SPI interface.

Write Protect Features for data memory

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable commands and automatic write disable after erase or program
- Software and Hardware (WP# pin) write protection using Status Register
- Write Protection using Power-down command
- Lock Down write protection for Status Register until the next power-up

Upon power-up or at power-down, the FM25NQ04TX will maintain a reset condition while VCC is below the threshold value of VWI, (See “**11.2.4 Power-up** Timing” and **Figure** 118). While reset, all operations are disabled and no commands are recognized. During power-up and after the VCC voltage exceeds VWI, all program and erase related commands are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register commands. Note that the chip select pin (CS#) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached. If needed a pull-up resister on CS# can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable command must be issued before a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register command will be accepted. After completing a program, erase or write command the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register command and setting the Status Register Protect (SRP0, SRP1) and Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits. These settings allow a portion as small as a 4KB sector or the entire memory array to be configured as read only. Used in conjunction with the Write Protect (WP#) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register section for further information. Additionally, the Power-down command offers an extra level of write protection as all commands are ignored except for the Release Power-down command.

7.1.1.2 Data memory write protection in RF interface

In RF interface, besides the above write protection methods, there is another read and write protection mechanism, using RF_DATA_WR_LOCK, RF_DATA_RD_LOCK and RF_DATA_PWD that is defined in data lock memory.

The default value of each byte of RF_DATA_PWD at delivery is 00h.

7.2 Data memory status register

Itag status registers can be read using the Read Tag Status Register command. Write access to the Status Register is controlled by the Tag Write Enable command and must be in CT_TAG_PWD authenticated state.

The Read Status Register-1, Status Register-2, Register-3, Register-4 and Register-5 commands can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, the state of write protection, Quad SPI setting, Security Sector lock status and Erase/Program Suspend status. The Write Status Register command can be used to configure the device write protection features, Quad SPI setting and Security Sector OTP lock. Write access to the Status Register-1~4 is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable command, and during Standard/Dual SPI operations, the WP# pin. Write access to Status Register-1 is controlled by data memory authenticated status, which requires contact interface password authentication. It should be noticed that Status Register-5 can only be changed from 0 to 1 in RF interface, even though in authenticated status.

Factory default for all Status Register bits are 0.

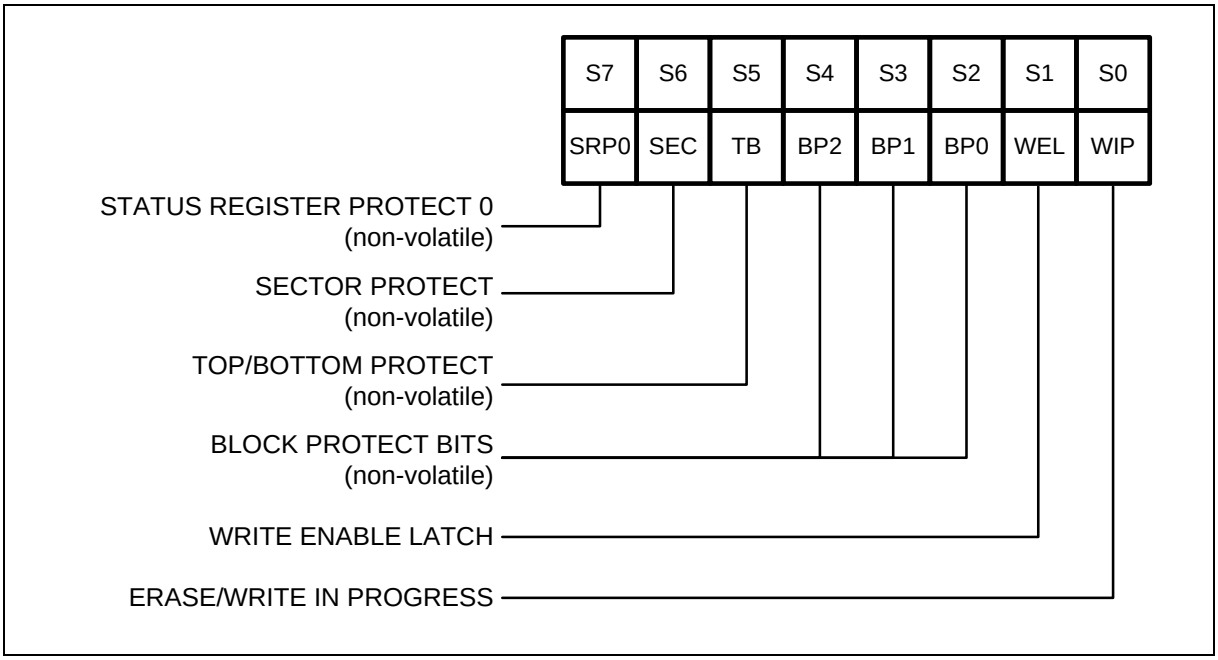


Figure 2 Status Register-1

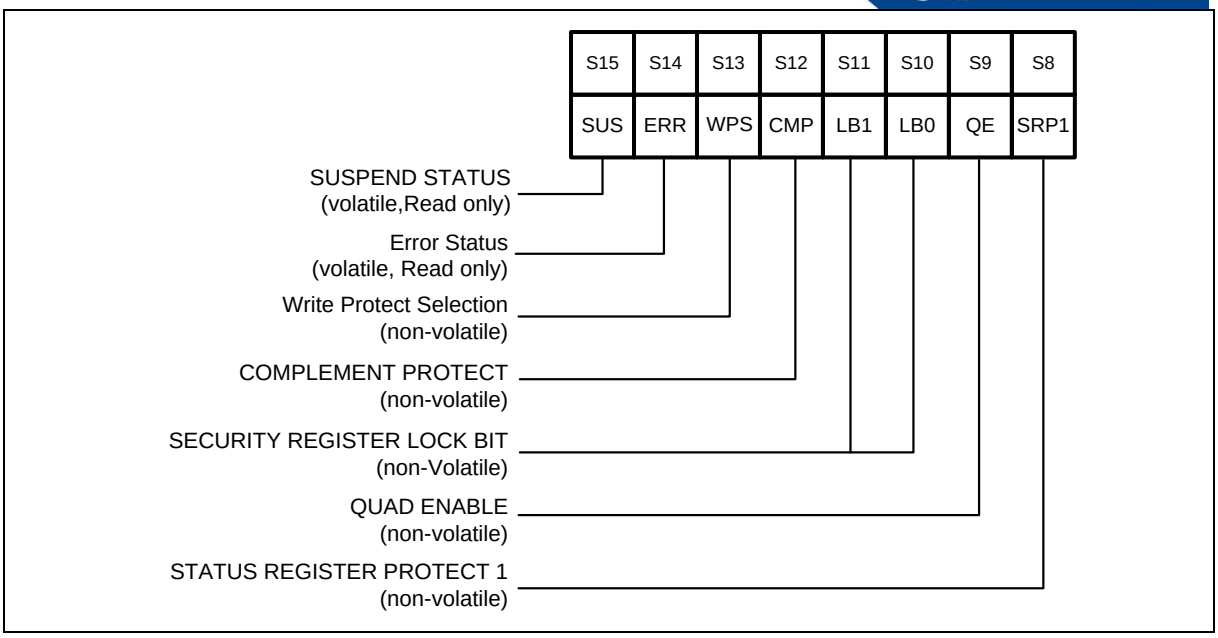


Figure 3 Status Register-2

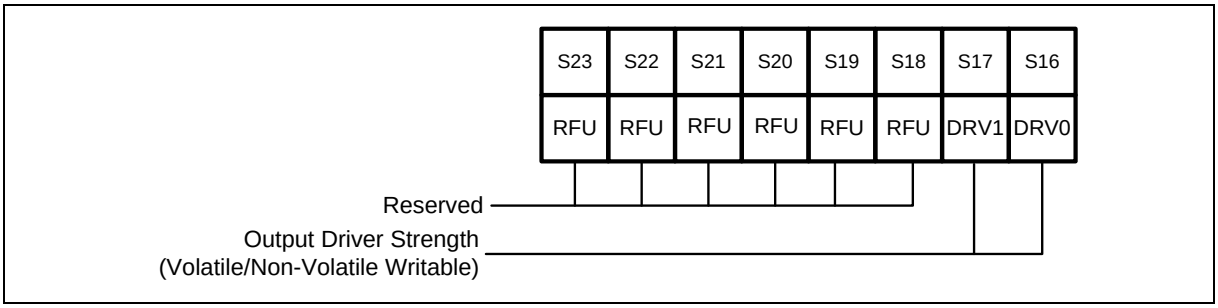


Figure 4 Status Register-3

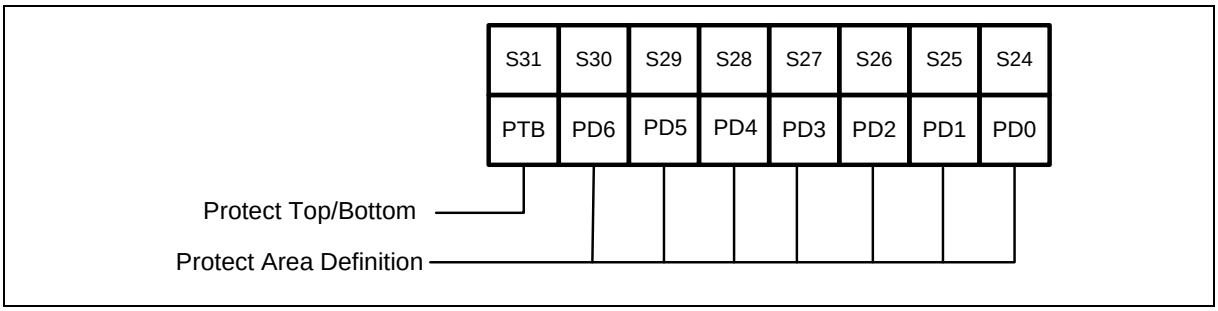


Figure 5 Status Register-4 (Volatile/Non-Volatile Writeable)

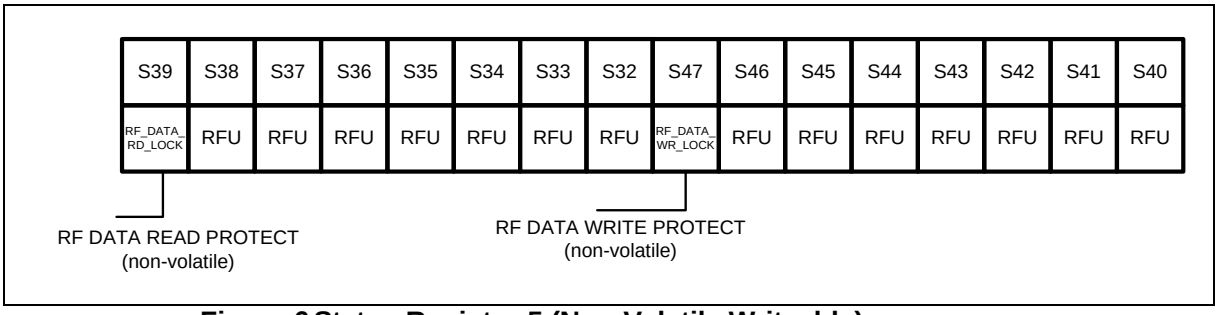


Figure 6 Status Register-5 (Non-Volatile Writeable)

7.2.1 WIP Bit

WIP is a read only bit in the status register (S0) that is set to a 1 state when the data memory is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Sector command. During this time the device will ignore further commands except for the Read Status Register and Erase/Program Suspend command (see t_W, t_{PP}, t_{SE}, t_{BE}, and t_{CE} in "11.2.3 AC Characteristics"). When the program, erase or write status register (or security sector) command has completed, the WIP bit will be cleared to a 0 state indicating the device is ready for further commands.

7.2.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Command to data memory. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following commands: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Sector and Program Security Sector.

7.2.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Command (see t_W in "11.2.3 AC Characteristics"). All, none or a portion of the memory array can be protected from Program and Erase commands (see Table 3 Status Register Memory Protection). The factory default setting for the Block Protection Bits is 0, none of the array protected.

7.2.4 Top/Bottom Block Protect (TB)

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in Table 3 Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Command depending on the state of the SRP0, SRP1 and WEL bits.

7.2.5 Sector/Block Protect (SEC)

The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in Table 3 Status Register Memory Protection table. The default setting is SEC=0.

7.2.6 Complement Protect (CMP)

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 4KB sector can be protected while the rest of the array is not; when CMP=1, the top 4KB sector will become unprotected while the rest of the array become read-only. Please refer to Table 3 Status Register Memory Protection table for details. The default setting is CMP=0.

7.2.7 Status Register Protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register (S8 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

Table 2 Status Register Protect bits

SRP1	SRP0	WP#	Status Register	Description
0	0	X	Software Protection	WP# pin has no control. The Status register can be written to after a Write Enable command, WEL=1. (Factory Default)
0	1	0	Hardware Protected	When WP# pin is low the Status Register locked and can not be written to.
0	1	1	Hardware Unprotected	When WP# pin is high the Status register is unlocked and can be written to after a Write Enable command, WEL=1.
1	0	X	Power Supply Lock-Down	Status Register is protected and can not be written to again until the next power-down, power-up cycle.(1)
1	1	X	One Time Program	Status Register is permanently protected and can not be written to.

Note:

1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.

7.2.8 Erase/Program Suspend Status (SUS)

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) command. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) command as well as a power-down, power-up cycle.

7.2.9 Error Bit (ERR)

The Error bit is a status flag, which shows the status of last Program/Erase operation. It will be set to "1", if the Program/Erase operation fails or the Program/Erase region is protected.

7.2.10 Security Sector Lock Bits (LB1,LB0)

The Security Register Lock Bit (LB1-0) are non-volatile One Time Program (OTP) bits in Status Register (S12,S11) that provide the write protect control and status to the Security Registers. The default state of LB1-0 is 0, Security Registers are unlocked. LB1-0 can be set to 1 individually using the Write Status Register command. LB1-0 are One Time Programmable (OTP), once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently.

7.2.11 Quad Enable (QE)

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI and QPI operation. When the QE bit is set to a 0 state (factory default), the WP# pin and HOLD# are enabled. When the QE bit is set to a 1, the Quad DQ_2 and DQ_3 pins are enabled, and WP# and HOLD# functions are disabled.

QE bit is required to be set to a 1 before issuing an "Enable QPI (38h)" to switch the device from Standard/Dual/Quad SPI to QPI, otherwise the command will be ignored. When the device is in QPI mode, QE bit will remain to be 1. A "Write Status Register" command in QPI mode cannot change QE bit from a "1" to a "0".

WARNING: If the WP# or HOLD# pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.

7.2.12 Write Protect Selection (WPS)

The WPS bit is used to select which Write Protect scheme should be used. When WPS=0, the device will use the combination of CMP, TB, SEC, BP[2:0] to protect a specific area of the memory array. When WPS=1, the device will utilize the Individual Sector Locks to protect any individual sector. The default value for all Individual Sector Lock bits is 1 upon device power on or after reset.

7.2.13 Protect Area Definition(PD6-PD0)

When WPS=1, PD6-PD0 bits are used to define which sector(s) cannot be Unlocked. See 7.2.14.

7.2.14 Protect Top/Bottom (PTB)

When WPS=1, the PTB bit is used to define Protect Area Definition in conjunction with PD6-PD0. Individual Sector Unlock(39h) command compares PTB/PD6-PD0 with input address, if input address is within Protect Area defined below, the command will be ignored and the specific sector will not be unlocked .

PTB	PD<6:0>	Sector protect bits cannot be unlocked
0	00	ALL Sector protect bits can be Unlocked
0	N(N>0)	N~127
1	N(N<127)	0~N
1	7F	ALL Sector protect bits can NOT be Unlocked

Note : when SR4≠00 or SR4≠FF, Global Sector Unlock(98h) command is ignored.

7.2.15 Reserved Bits (RFU)

There are a few reserved Status Register bits that may be read out as a “0” or “1”.It is recommended to ignore the values of those bits. During a “Write Status Register” command, the Reserved Bits can be written as “0”, but there will not be any effects.

7.2.16 Output driver strength (DRV1, DRV0)

The DRV1 & DRV0 bits are used to determine the output driver strength.

DRV1, DRV0	Driver Strength
0,0	100%
0,1	75%
1,0	50%
1,1	25%

7.2.17 Status Register Memory Protection(WPS=0, CMP=0)

Table 3 Status Register Memory Protection (CMP=0)

STATUS REGISTER					FM25NQ04TX (4M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	7	070000h – 07FFFFh	64KB	Upper 1/8
0	0	0	1	0	6 and 7	060000h – 07FFFFh	128KB	Upper 1/4
0	0	0	1	1	4 thru 7	040000h – 07FFFFh	256KB	Upper 1/2
0	1	0	0	1	0	000000h – 00FFFFh	64KB	Lower 1/8

STATUS REGISTER					FM25NQ04TX (4M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
0	1	0	1	0	0 and 1	000000h – 01FFFFh	128KB	Lower 1/4
0	1	0	1	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/2
0	X	1	X	X	0 thru 7	000000h – 07FFFFh	512KB	ALL
1	0	0	0	1	7	07F000h – 07FFFFh	4KB	Upper 1/128
1	0	0	1	0	7	07E000h – 07FFFFh	8KB	Upper 1/64
1	0	0	1	1	7	07C000h – 07FFFFh	16KB	Upper 1/32
1	0	1	0	X	7	078000h – 07FFFFh	32KB	Upper 1/16
1	0	1	1	0	7	078000h – 07FFFFh	32KB	Upper 1/16
1	1	0	0	1	0	000000h – 000FFFh	4KB	Lower 1/128
1	1	0	1	0	0	000000h – 001FFFh	8KB	Lower 1/64
1	1	0	1	1	0	000000h – 003FFFh	16KB	Lower 1/32
1	1	1	0	X	0	000000h – 007FFFh	32KB	Lower 1/16
1	1	1	1	0	0	000000h – 007FFFh	32KB	Lower 1/16
1	X	1	1	1	63	000000h – 07FFFFh	512KB	ALL

7.2.18 Status Register Memory Protection(WPS=0, CMP=1)

Table 4 Status Register Memory Protection (CMP=1)

STATUS REGISTER					FM25NQ04TX (4M-BIT) MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION
X	X	0	0	0	0 thru 7	000000h – 07FFFFh	512KB	All
0	0	0	0	1	0 thru 6	000000h – 06FFFFh	448KB	Lower 7/8
0	0	0	1	0	0 thru 5	000000h – 05FFFFh	384KB	Lower 3/4
0	0	0	1	1	0 thru 3	000000h – 03FFFFh	256KB	Lower 1/2
0	1	0	0	1	1 thru 7	010000h – 07FFFFh	448KB	Upper 1/8
0	1	0	1	0	2 thru 7	020000h – 07FFFFh	384KB	Upper 1/4
0	1	0	1	1	4 thru 7	040000h – 07FFFFh	256KB	Upper 1/2
0	X	1	X	X	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 7	000000h – 07EFFFh	508KB	Lower 127/128
1	0	0	1	0	0 thru 7	000000h – 07DFFFh	504KB	Lower 63/64
1	0	0	1	1	0 thru 7	000000h – 07BFFFh	496KB	Lower 31/32
1	0	1	0	X	0 thru 7	000000h – 077FFFh	480KB	Lower 15/16
1	0	1	1	0	0 thru 7	000000h – 077FFFh	480KB	Lower 15/16
1	1	0	0	1	0	001000h – 07FFFFh	4KB	Upper 127/128
1	1	0	1	0	0	002000h – 07FFFFh	8KB	Upper 63/64
1	1	0	1	1	0	004000h – 07FFFFh	16KB	Upper 31/32
1	1	1	0	X	0	008000h – 07FFFFh	32KB	Upper 15/16
1	1	1	1	0	0	008000h – 07FFFFh	32KB	Upper 15/16
X	X	1	1	1	NONE	NONE	NONE	NONE

7.2.19 Status Register Memory Protection (WPS=1)

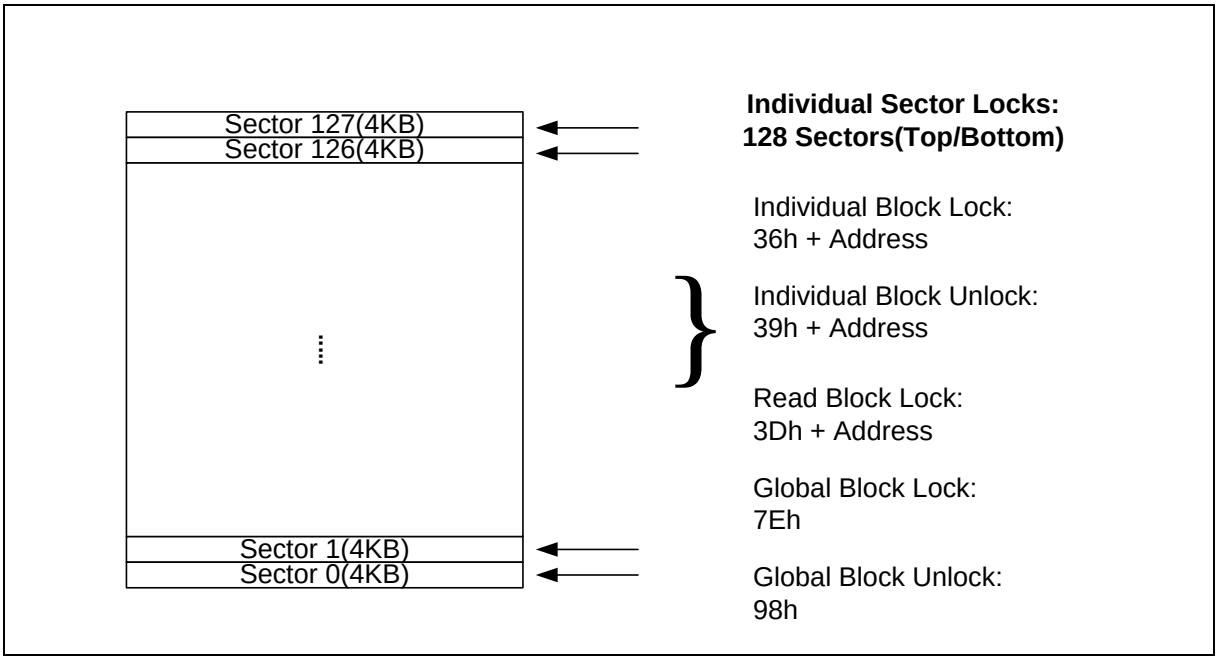


Figure 7 Individual Sector Locks

7.2.20 RF interface data memory read lock bit (RF_DATA_RD_LOCK)

RF_DATA_RD_LOCK is a register that locks the read access of data memory in RF interface.

In RF interface, the read access of RF_DATA_RD_LOCK doesn't need authentication of RF password (RF_DATA_PWD). However, the write access must be in RF_DATA_PWD authenticated state.

RF_DATA_RD_LOCK does not impact read access of contact interface.

The default value of each bit of RF_DATA_RD_LOCK at delivery is 0b.

7.2.21 RF interface data memory write lock bit (RF_DATA_WR_LOCK)

RF_DATA_WR_LOCK is a register that locks the write access of data memory in RF interface besides the write protection configured in data memory status register1 & 2.

In RF interface, the read access of RF_DATA_WR_LOCK doesn't need authentication of RF password (RF_DATA_PWD). However, the write access must be in RF_DATA_PWD authenticated state.

RF_DATA_RD_LOCK does not impact read access of contact interface.

The default value of each bit of RF_DATA_RD_LOCK at delivery is 0b.

7.3 Tag memory

In FM25NQ04Tx, there's a tag memory to ensure NFC Forum Type 2 Tag operation. It can be accessed by SPI interface, with SPI tag command, using 2 bytes of byte address. The address range varies according to tag type, refers to Table 5-8.

The tag memory is organized in pages of 16 bytes each when accessed by SPI interface. Meanwhile, the tag memory is organized in blocks of 4 bytes each when accessed by RF interface. Each block can be individually accessed by tag command.

For FM25NQ04T1 variant, the tag memory size is 180 bytes, including 144 bytes user memory. NFC Tag is organized in blocks with 4 bytes. Each block can be individually accessed by tag command.

Table 5 Tag memory organization of FM25NQ04T1

Contact CMD		Tag CMD		Byte number inside block				Description
Page addr.	Byte addr.	Block addr. Hex.	Block addr. Dec.	0	1	2	3	
000h ~ 003h	0000h	00h	0	UID0/RFU	UID1/RFU	UID2/RFU	BCC0/RFU	UID and static lock bytes
	0004h	01h	1	UID3/RFU	UID4/RFU	UID5/RFU	UID6/RFU	
	0008h	02h	2	BCC1/RFU	Internal/RFU	Lock_byte[0]	Lock_byte[1]	
	000Ch	03h	3	Capability Container (CC)				CC
	0010h	04h	4	Static Data Area (Block 04h-0Fh, total 12 blocks)				User data
	…	…	…					
	003Ch	0Fh	15					
004h ~ 00Bh	0040h	10h	16	Dynamic Data Area (Block 10h~2Bh, total 24 blocks)				
	…	…	…					
	009Ch	27h	39					
	00A0h	28h	40	Dynamic Lock Bytes				Dynamic Lock Bytes
	00A4h	29h	41	FDP & MIRROR	RFU	MIRROR_BLOCK	AUTH0	Configuration
	00A8h	2Ah	42	ACCESS	RFU			
	00ACh	2Bh	43	PWD				
	00B0h	2Ch	44	PACK		RFU		
See 7.4		2Dh	45	EH_FD_CFG	GPO_CFG	RFU		Tag system

For FM25NQ04T2, the tag memory size is 540 bytes, including 504 bytes user memory. NFC Tag is organized in blocks with 4 bytes. Each block can be individually accessed by tag command.

Table 6 Tag memory organization of FM25NQ04T2

Contact CMD		Tag CMD		Byte number inside block				Description
Page addr.	Byte addr.	Block addr. Hex.	Block addr. Dec.	0	1	2	3	
000h ~ 003h	0000h	00h	0	UID0/RFU	UID1/RFU	UID2/RFU	BCC0/RFU	UID and static lock bytes
	0004h	01h	1	UID3/RFU	UID4/RFU	UID5/RFU	UID6/RFU	
	0008h	02h	2	BCC1/RFU	Internal/RFU	Lock_byte[0]	Lock_byte[1]	
	000Ch	03h	3	Capability Container (CC)				CC
	0010h	04h	4	Static Data Area (Block 04h-0Fh, total 12 blocks)				User data
	…	…	…					
	003Ch	0Fh	15					
004h ~ 021h	0040h	10h	16	Dynamic Data Area (Block 10h~81h, total 114 blocks)				
	…	…	…					
	0204h	81h	129					
	0208h	82h	130	Dynamic Lock Bytes				Dynamic Lock Bytes
	020Ch	83h	131	FDP & MIRROR	RFU	MIRROR_BLOCK	AUTH0	Configuration
	0210h	84h	132	ACCESS	RFU			
	0214h	85h	133	PWD				
	021Ch	86h	134	PACK		RFU		
See 7.4		87h	135	EH_FD_CFG	GPO_CFG	RFU		Tag system

For FM25NQ04T3, the tag memory size is 924 bytes, including 888 bytes user memory. NFC Tag

is organized in blocks with 4 bytes. Each block can be individually accessed by tag command.

Table 7 Tag memory organization of FM25NQ04T3

Contact CMD		Tag CMD		Byte number inside block				Description
Page addr.	Byte addr.	Block addr.		0	1	2	3	
		Hex.	Dec.					
000h ~ 003h	0000h	00h	0	UID0/RFU	UID1/RFU	UID2/RFU	BCC0/RFU	UID and static lock bytes
	0004h	01h	1	UID3/RFU	UID4/RFU	UID5/RFU	UID6/RFU	
	0008h	02h	2	BCC1/RFU	Internal/RFU	Lock_byte[0]	Lock_byte[1]	
	000Ch	03h	3	Capability Container (CC)				CC
	0010h	04h	4	Static Data Area (Block 04h-0Fh, total 12 blocks)				User data
	…	…	…					
	003Ch	0Fh	15					
004h ~ 039h	0040h	10h	16	Dynamic Data Area (Block 10h~E1h, total 210 blocks)				
	…	…	…					
	0384h	E1h	225					
	0388h	E2h	226	Dynamic Lock Bytes				Dynamic Lock Bytes
	038Ch	E3h	227	FDP & MIRROR	RFU	MIRROR_BLOCK	AUTH0	Configuration
	0390h	E4h	228	ACCESS	RFU			
	0394h	E5h	229	PWD				
	0398h	E6h	230	PACK		RFU		
See 7.4		E7h	231	EH_FD_CFG	GPO_CFG	RFU		Tag system

For FM25NQ04T4, the tag memory size is 1920 bytes, including 1884 bytes user memory. NFC Tag is organized in blocks with 4 bytes. Each block can be individually accessed by tag command.

Table 8 Tag memory organization of FM25NQ04T4

Contact CMD		Tag CMD			Byte number inside block				Description
Page addr.	Byte addr.	Sector addr.	Block addr.		0	1	2	3	
			Hex.	Dec.					
000h ~ 003h	0000h	0	00h	0	UID0/RFU	UID1/RFU	UID2/RFU	BCC0/RFU	UID and static lock bytes
	0004h		01h	1	UID3/RFU	UID4/RFU	UID5/RFU	UID6/RFU	
	0008h		02h	2	BCC1/RFU	Internal/RFU	Lock_byte[0]	Lock_byte[1]	
	000Ch		03h	3	Capability Container (CC)				CC
	0010h		04h	4	Static Data Area (Block 04h-0Fh, total 12 blocks)				User data
	…		…	…					
	003Ch		0Fh	15					
004h ~ 077h	0040h		10h	16	Dynamic Data Area (Sector 0 Block 10h~Sector 1Block DAh, total 459 Blocks)				
	…		…	…					
	03FCh		FFh	255					
	0400h	1	00h	0					
	…		…	…					
	0768h		DAh	218					
	076Ch		DBh	219	Dynamic Lock Bytes				Dynamic Lock Bytes
	0770h		DCh	220	FDP & MIRROR	RFU	MIRROR_BLOCK	AUTH0	Configuration
	0774h		DDh	221	ACCESS	RFU		SEC_CFG	
	0778h		DEh	222	PWD				
	077Ch		DFh	223	PACK		RFU		
See 7.4			E0	224	EH_FD_CFG	GPO_CFG	RFU		Tag system

7.3.1 Read only bytes(0000h~0009h)

In RF interface, these 10 bytes are the mirror of UID, which are read only. Any read operation replies tag UID. In contact interface, these 10 bytes can be written to any data, and be readout. But it can not change the reply of read operation of RF interface.

Remark: The real UID and anticollision operation will not be influenced if these bytes are changed by contact interface.

7.3.2 Static lock bytes(000Ah~000Bh)

In RF interface, the bits of byte 2 and byte 3 of block 02h represent the field programmable read-only locking mechanism. Each block from 03h (CC) to 0Fh can be individually locked by setting the corresponding locking bit Lx to logic 1 to prevent further write access. After locking, the corresponding block becomes read-only memory.

The three least significant bits of lock byte 0 are the block-locking bits. Bit 2 deals with block 0Ah to 0Fh, bit 1 deals with block 04h to 09h and bit 0 deals with block 03h (CC). Once the block-locking bits are set Logic 1, the locking configuration for the corresponding memory area is frozen.

Table 9 Static lock bytes of FM25NQ04Tx

Field	Byte No.	Bit number inside byte							
		7	6	5	4	3	2	1	0
Static lock bytes	0	L7	L6	L5	L4	LCC	BL15-10	BL9-4	BLCC
	1	L15	L14	L13	L12	L11	L10	L9	L8

Remark: Lx locks Block x to read-only; BLx-y blocks further locking for the memory area x-y.

For example if BL15-10 is set to logic 1, then bits L15 to L10 (lock byte 1, bit [7:2]) can no longer be changed.

The so called static locking and block-locking bits are set by a WRITE or COMPATIBILITY_WRITE command to block 02h. Bytes 2 and 3 of the WRITE or COMPATIBILITY_WRITE command and the contents of the lock bytes are bit-wise OR'ed and the result then becomes the new content of the lock bytes. This process is irreversible. If a bit is set to logic 1, it cannot be changed back to logic 0. The contents of bytes 0 and 1 of block 02h are unaffected by the corresponding data bytes of the WRITE or COMPATIBILITY_WRITE command.

In contact interface, static lock bytes don't affect the write access of tag memory.

The default value of the static lock bytes at delivery is 00h.

7.3.3 Dynamic Lock Bytes

In RF interface, to lock the blocks starting at block address 10h and onwards, the so called dynamic lock bytes are used.

For FM25NQ04T1 variant, those three lock bytes cover the memory area of 96 data bytes. The granularity is 2 blocks, compared to a single block for the first 64 bytes as shown in Table 10.

For FM25NQ04T2 variant, those four lock bytes cover the memory area of 456 data bytes. The granularity is 16 blocks, compared to a single block for the first 64 bytes as shown in Table 11.

For FM25NQ04T3 variant, those four lock bytes cover the memory area of 840 data bytes. The granularity is 16 blocks, compared to a single block for the first 64 bytes as shown in Table 12.

For FM25NQ04T4 variant, those four lock bytes cover the memory area of 1836 data bytes. The granularity is 32 blocks, compared to a single block for the first 64 bytes as shown in Table 13.

Remark: Set all bits marked with RFU to 0, when writing to the dynamic lock bytes.

Table 10 Dynamic Lock Byte of FM25NQ04T1

Field	Byte No.	Bit number inside byte							
		7	6	5	4	3	2	1	0
Dynamic lock byte	0	L30-31	L28-29	L26-27	L24-25	L22-23	L20-21	L18-19	L16-17
	1	RFU	RFU	RFU	RFU	L38-39	L36-37	L34-35	L32-33
	2	RFU	RFU	BL36-39	BL32-25	BL28-31	BL24-27	BL20-23	BL16-19
	3	RFU							

Remark: Lx-y locks Block x-y to read-only; BLx-y blocks further locking for Block x-y.

Table 11 Dynamic Lock Byte of FM25NQ04T2

Field	Byte No.	Bit number inside byte							
		7	6	5	4	3	2	1	0
Dynamic lock byte	0	L128-129	L112-127	L96-111	L80-95	L64-79	L48-63	L32-47	L16-31
	1	RFU							
	2	RFU				BL112-129	BL80-111	BL48-79	BL16-47
	3	RFU							

Remark: Lx-y locks Block x-y to read-only. BLx-y blocks further locking for Block x-y.

Table 12 Dynamic Lock Byte of FM25NQ04T3

Field	Byte No.	Bit number inside byte							
		7	6	5	4	3	2	1	0
Dynamic lock byte	0	L128-143	L112-127	L96-111	L80-95	L64-79	L48-63	L32-47	L16-31
	1	RFU		L224-225	L208-223	L192-207	L176-191	L160-175	L144-159
	2	RFU	BL208-225	BL176-207	BL144-175	BL112-143	BL80-111	BL48-79	BL16-47
	3	RFU							

Remark: Lx-y locks Block x-y to read-only; BLx-y blocks further locking for Block x-y.

Table 13 Dynamic Lock Byte of FM25NQ04T4

Field	Byte No.	Bit number inside byte							
		7	6	5	4	3	2	1	0
Dynamic lock byte	0	L240-271	L208-239	L176-207	L144-175	L112-143	L80-111	L48-79	L16-47
	1	RFU	L464-474	L432-463	L400-431	L368-399	L336-367	L304-335	L272-303
	2	BL464-474	BL400-463	BL336-399	BL272-335	BL208-271	BL144-207	BL80-143	BL16-79
	3	RFU							

Remark: Lx-y locks Block x-y to read-only; BLx-y blocks further locking for Block x-y. There are 459 dynamic data blocks, 240 blocks in sector 0 and 219 blocks in sector 1, respectively.

Dynamic lock bytes of the WRITE or COMPATIBILITY_WRITE command and the current contents of the dynamic lock bytes is bit-wise OR'ed. The result is the new dynamic lock bytes contents. This process is irreversible. Once a bit is set to logic 1, it cannot be changed back to logic 0.

In contact interface, dynamic lock bytes don't affect the write access of tag memory.

The default value of dynamic lock bytes at delivery is 00h.

7.3.4 Capability Container (CC) bytes(000Ch~000Fh)

The Capability Container CC (block 3) is programmed during the IC production according to the NFC Forum Type 2 Tag specification. These bytes may be bit-wise modified by a WRITE or COMPATIBILITY_WRITE command.

Default value of FM25NQ04T1 CC bytes

1110 0001	0001 0000	0001 01010	0000 0000

WRITE command to block 03h

0000 0000	0000 0000	0000 0000	0000 1111

Result in block 03h (read-only state)

1110 0001	0001 0000	0001 0010	0000 1111

Figure 8 the example of CC bytes write

The parameter bytes of the WRITE command and the current contents of the CC bytes are bit-wise OR'ed. The result is the new CC byte contents. This process is irreversible. Once a bit is set to logic 1, it cannot be changed back to logic 0.

The default values of the CC bytes at delivery are defined in Section 7.3.6.

7.3.5 Data blocks

Blocks 04h to 27h for FM25NQ04T1, blocks 04h to 81h for FM25NQ04T2, blocks 04h to E1h for FM25NQ04T3 and blocks 04h of sector 0 to DAh of sector 1 for FM25NQ04T4 are the user memory read/write area. The access to a part of the user memory area can be restricted using password verification. See Section 7.3.7 for further details.

The default values of the data blocks at delivery are defined in Section 7.3.6.

7.3.6 CC and Data blocks content at delivery

The tag memory of FM25NQ04Tx are pre-programmed to the initialized state according to the NFC Forum Type 2 Tag specification as defined in Table 14, Table 15, Table 16 and Table 17.

Table 14 Memory content at delivery of FM25NQ04T1

Contact CMD		Tag CMD	Byte number inside block			
Page addr.	**Byte addr.**	**Block addr.**	**0**	**1**	**2**	**3**
000h	000Ch	03h	E1h	10h	12h	00h
	0010h	04h	01h	03h	A0h	0Ch
	0014h	05h	34h	03h	03h	D0h
	0018h	06h	00h	00h	FEh	00h

Table 15 Memory content at delivery of FM25NQ04T2

Contact CMD		Tag CMD	Byte number inside block			
Page addr.	Byte addr.	Block addr.	0	1	2	3
000h	000Ch	03h	E1h	10h	3Fh	00h
	0010h	04h	01h	03h	88h	08h
	0014h	05h	66h	03h	03h	D0h
	0018h	06h	00h	00h	FEh	00h

Table 16 Memory content at delivery of FM25NQ04T3

Contact CMD		Tag CMD	Byte number inside block			
Page addr.	Byte addr.	Block addr.	0	1	2	3
000h	000Ch	03h	E1h	10h	6Fh	00h
	0010h	04h	01h	03h	E8h	0Eh
	0014h	05h	66h	03h	03h	D0h
	0018h	06h	00h	00h	FEh	00h

Table 17 Memory content at delivery of FM25NQ04T4

Contact CMD		Tag CMD	Byte number inside block			
Page addr.	Byte addr.	Block addr.	0	1	2	3
000h	000Ch	03h	E1h	10h	6Fh	00h
	0010h	04h	01h	03h	E8h	0Eh
	0014h	05h	66h	03h	03h	D0h
	0018h	06h	00h	00h	FEh	00h

The access to a part of the user memory area of tag memory can be restricted using password verification. Please see Section 7 for further details.

7.3.7 Configuration

Blocks 29h to 2Ah for FM25NQ04T1 variant, blocks 83h to 84h for FM25NQ04T2 variant, blocks E3h to E4h for FM25NQ04T3 variant and blocks DCh to DDh of sector 1 variant are used to configure the memory access restriction and to configure the UID ASCII mirror feature.

Blocks 2Bh to 2Ch for FM25NQ04T1 variant, blocks 85h to 86h for FM25NQ04T2 variant, blocks E5h to E6h for FM25NQ04T3 variant and blocks DEh to DFh of sector 1 variant are used as password and PACK.

Table 18 MIRROR_BYTE configuration

Byte address	Block address	Field	Bit number inside byte							
			7	6	5	4	3	2	1	0
00A4h/ 020Ch/ 038Ch/ 0770h	29h/ 83h/ E3h/ DCh	FDP & MIRROR	MIRROR_CONF		MIRROR_BYTE		SLEEP_EN	STRG_MOD_EN	FDP_CONF	

Remark: Byte/Block address is for FM25NQ04T1, FM25NQ04T2 and FM25NQ04T3 individually.

Table 19 ACCESS configuration

Byte address	Block address	Field	Bit number inside byte							
			7	6	5	4	3	2	1	0
03A8h 0210h 0390h 0774h	2Ah 84h E4h DDh	ACCESS	PROT	CFGLCK	RFU	NFC_CNT_EN	NFC_CNT_PWD_PROT_EN	AUTHLIM		

Remark: Byte/Block address is for FM25NQ04T1, FM25NQ04T2 and FM25NQ04T3 individually.

Table 20 SEC_CFG configuration

Byte address	Block address	Field	Bit number inside byte							
			7	6	5	4	3	2	1	0
0777h	DDh	ACCESS	RFU						MIRRORS	AUTHS

Remark: Byte/Block address is for FM25NQ04T4, this configuration makes sense only for FM25NQ04T4.

Table 21 TAG configuration parameter description

FM25NQ04T1

Part number	Byte address	Block address	Field	Bit	Default values	description
FM25NQ04T1	00A4h	29h	MIRROR_CONF	2	00b	Defines which ASCII mirror shall be used, if the ASCII mirror is enabled by a valid MIRROR_BLOCK byte 00b ... no ASCII mirror 01b ... UID ASCII mirror 10b … Counter mirror 11b … UID & counter mirror
FM25NQ04T1	00A4h	29h	MIRROR_BYTE	2	00b	The 2 bits define the byte position within the block defined by the MIRROR_BLOCK byte (beginning of ASCII mirror)
FM25NQ04T1	00A4h	29h	SLEEP_EN	1	0b	Enables the SLEEP mode function
FM25NQ04T1	00A4h	29h	STRG_MOD_EN	1	0b	Controls the tag modulation strength - by default strong modulation is enabled
FM25NQ04T1	00A4h	29h	FDP_CONF	2	11h	FDP CONF defines the configuration of the Field detect pin 00b ... enabled by first State-of-Frame (start of communication) 01b... enabled by halt with previous read operation 10b... enabled by selection of the tag 11b... enabled by field presence
FM25NQ04T1	00A6h	29h	MIRROR_BLO	8	00h	MIRROR_BLOCK defines the

Part number	Byte address	Block address	Field	Bit	Default values	description
			CK			bolck for the beginning of the ASCII mirroring A value >03h enables the ASCII mirror feature 04h-24h ... valid MIRROR_BLOCK values for FM25NQ04T1 (UID ASCII mirror) 04h-26h ... valid MIRROR_BLOCK values for FM25NQ04T1 (NFC counter mirror only) 04h-22h ... valid MIRROR_BLOCK values for FM25NQ04T1 (both UID and NFC counter mirror)
FM25NQ04T1	00A7h	29h	AUTH0	8	FFh	AUTH0 defines the block address from which the password verification is required. Valid address range for byte AUTH0 is from 00h to FFh. If AUTH0 is set to a block address which is higher than the last block from the user configuration, the password protection is effectively disabled.
FM25NQ04T1	00A8h	2Ah	PROT	1	0b	One bit inside the ACCESS byte defining the memory protection 0b ... write access is protected by the password verification 1b ... read and write access is protected by the password verification
FM25NQ04T1	00A8h	2Ah	CFGLCK	1	0b	Write locking bit for the user configuration excluding the PWD and PACK 0b ... user configuration open to write access 1b ... user configuration permanently locked against write access
FM25NQ04T1	00A8h	2Ah	NFC_CNT_EN	1	0b	Enables the NFC counter 0b ... disabled 1b ... enabled
FM25NQ04T1	00A8h	2Ah	NFC_CNT_PWD_PROT_EN	1	0b	enables the password protection to read out and mirror the NFC counter 0b ... the protection is disabled 1b ... the protection is enabled
FM25NQ04T1	00A8h	2Ah	AUTHLIM	3	000b	Limitation of negative password verification attempts

Part number	Byte address	Block address	Field	Bit	Default values	description
						000b ... limiting of negative password verification attempts disabled 001b-111b ... maximum number of negative password verification attempts

FM25NQ04T2

Part number	Byte address	Block address	Field	Bit	Default values	description
FM25NQ04T2	020Ch	83h	MIRROR_CONF	2	00b	Defines which ASCII mirror shall be used, if the ASCII mirror is enabled by a valid MIRROR_BLOCK byte 00b ... no ASCII mirror 01b ... UID ASCII mirror 10b … Counter mirror 11b … UID & counter mirror
FM25NQ04T2	020Ch	83h	MIRROR_BYTE	2	00b	The 2 bits define the byte position within the block defined by the MIRROR_BLOCK byte (beginning of ASCII mirror)
FM25NQ04T2	020Ch	83h	SLEEP_EN	1	0b	Enables the SLEEP mode function
FM25NQ04T2	020Ch	83h	STRG_MOD_EN	1	0b	Controls the tag modulation strength - by default strong modulation is enabled
FM25NQ04T2	020Ch	83h	FDP_CONF	2	11h	FDP CONF defines the configuration of the Field detect pin 00b ... enabled by first State-of-Frame (start of communication) 01b... enabled by halt with previous read operation 10b... enabled by selection of the tag 11b... enabled by field presence
FM25NQ04T2	020Eh	83h	MIRROR_BLOCK	8	00h	MIRROR_BLOCK defines the block for the beginning of the ASCII mirroring A value >03h enables the ASCII mirror feature 04h-7Eh ... valid MIRROR_BLOCK values for FM25NQ04T2 (UID ASCII mirror) 04h-80h ... valid MIRROR_BLOCK values for FM25NQ04T2 (NFC counter mirror only) 04h-7Ch ... valid

Part number	Byte address	Block address	Field	Bit	Default values	description
						MIRROR_BLOCK values for FM25NQ04T2 (both UID and NFC counter mirror)
FM25NQ04T2	020Fh	83h	AUTH0	8	FFh	AUTH0 defines the block address from which the password verification is required. Valid address range for byte AUTH0 is from 00h to FFh. If AUTH0 is set to a block address which is higher than the last block from the user configuration, the password protection is effectively disabled.
FM25NQ04T2	0210h	84h	PROT	1	0b	One bit inside the ACCESS byte defining the memory protection 0b ... write access is protected by the password verification 1b ... read and write access is protected by the password verification
FM25NQ04T2	0210h	84h	CFGLCK	1	0b	Write locking bit for the user configuration excluding the PWD and PACK 0b ... user configuration open to write access 1b ... user configuration permanently locked against write access
FM25NQ04T2	0210h	84h	NFC_CNT_EN	1	0b	Enables the NFC counter 0b ... disabled 1b ... enabled
FM25NQ04T2	0210h	84h	NFC_CNT_PWD_PROT_EN	1	0b	enables the password protection to read out and mirror the NFC counter 0b ... the protection is disabled 1b ... the protection is enabled
FM25NQ04T2	0210h	84h	AUTHLIM	3	000b	Limitation of negative password verification attempts 000b ... limiting of negative password verification attempts disabled 001b-111b ... maximum number of negative password verification attempts

FM25NQ04T3

Part number	Byte address	Block address	Field	Bit	Default values	description
FM25NQ04T3	038Ch	E3h	MIRROR_CONF	2	00b	Defines which ASCII mirror shall be used, if the ASCII mirror is enabled by a valid MIRROR_BLOCK byte 00b ... no ASCII mirror 01b ... UID ASCII mirror 10b … Counter mirror 11b … UID & counter mirror
FM25NQ04T3	038Ch	E3h	MIRROR_BYTE	2	00b	The 2 bits define the byte position within the block defined by the MIRROR_BLOCK byte (beginning of ASCII mirror)
FM25NQ04T3	038Ch	E3h	SLEEP_EN	1	0b	Enables the SLEEP mode function
FM25NQ04T3	038Ch	E3h	STRG_MOD_EN	1	0b	Controls the tag modulation strength - by default strong modulation is enabled
FM25NQ04T3	038Ch	E3h	FDP_CONF	2	11h	FDP CONF defines the configuration of the Field detect pin 00b ... enabled by first State-of-Frame (start of communication) 01b... enabled by halt with previous read operation 10b... enabled by selection of the tag 11b... enabled by field presence
FM25NQ04T3	038Eh	E3h	MIRROR_BLOCK	8	00h	MIRROR_BLOCK defines the block for the beginning of the ASCII mirroring A value >03h enables the ASCII mirror feature 04h-DEh ... valid MIRROR_BLOCK values for FM25NQ04T3 (UID ASCII mirror) 04h-E0h ... valid MIRROR_BLOCK values for FM25NQ04T3 (NFC counter mirror only) 04h-DCh ... valid MIRROR_BLOCK values for FM25NQ04T3 (both UID and NFC counter mirror)
FM25NQ04T3	038Fh	E3h	AUTH0	8	FFh	AUTH0 defines the block address from which the password verification is required. Valid address range for byte AUTH0 is from 00h to FFh.

Part number	Byte address	Block address	Field	Bit	Default values	description
						If AUTH0 is set to a block address which is higher than the last block from the user configuration, the password protection is effectively disabled.
FM25NQ04T3	0390h	E4h	PROT	1	0b	One bit inside the ACCESS byte defining the memory protection 0b ... write access is protected by the password verification 1b ... read and write access is protected by the password verification
FM25NQ04T3	0390h	E4h	CFGLCK	1	0b	Write locking bit for the user configuration excluding the PWD and PACK 0b ... user configuration open to write access 1b ... user configuration permanently locked against write access
FM25NQ04T3	0390h	E4h	NFC_CNT_EN	1	0b	Enables the NFC counter 0b ... disabled 1b ... enabled
FM25NQ04T3	0390h	E4h	NFC_CNT_PWD_PROT_EN	1	0b	enables the password protection to read out and mirror the NFC counter 0b ... the protection is disabled 1b ... the protection is enabled
FM25NQ04T3	0390h	E4h	AUTHLIM	3	000b	Limitation of negative password verification attempts 000b ... limiting of negative password verification attempts disabled 001b-111b ... maximum number of negative password verification attempts

FM25NQ04T4

Part number	Byte address	Block address	Field	Bit	Default values	description
FM25NQ04T4	0770h	E3h	MIRROR_CONF	2	00b	Defines which ASCII mirror shall be used, if the ASCII mirror is enabled by a valid MIRROR_BLOCK byte 00b ... no ASCII mirror 01b ... UID ASCII mirror 10b … Counter mirror 11b … UID & counter mirror
FM25NQ04T4	0770h	E3h	MIRROR_BYTE	2	00b	The 2 bits define the byte position within the block defined by the MIRROR_BLOCK byte

Part number	Byte address	Block address	Field	Bit	Default values	description
						(beginning of ASCII mirror)
FM25NQ04T4	0770h	E3h	SLEEP_EN	1	0b	Enables the SLEEP mode function
FM25NQ04T4	0770h	E3h	STRG_MOD_EN	1	0b	Controls the tag modulation strength - by default strong modulation is enabled
FM25NQ04T4	0770h	E3h	FDP_CONF	2	11h	FDP CONF defines the configuration of the Field detect pin 00b ... enabled by first State-of-Frame (start of communication) 01b... enabled by halt with previous read operation 10b... enabled by selection of the tag 11b... enabled by field presence
FM25NQ04T4	0772h	E3h	MIRROR_BLOCK	8	00h	MIRROR_BLOCK defines the block for the beginning of the ASCII mirroring A value >03h enables the ASCII mirror feature 04h-DEh ... valid MIRROR_BLOCK values for FM25NQ04T4 (UID ASCII mirror) 04h-E0h ... valid MIRROR_BLOCK values for FM25NQ04T4 (NFC counter mirror only) 04h-DCh ... valid MIRROR_BLOCK values for FM25NQ04T4 (both UID and NFC counter mirror)
FM25NQ04T4	0773h	E3h	AUTH0	8	FFh	AUTH0 defines the block address from which the password verification is required. Valid address range for byte AUTH0 is from 00h to FFh. If AUTH0 is set to a block address which is higher than the last block from the user configuration, the password protection is effectively disabled.
FM25NQ04T4	0774h	E4h	PROT	1	0b	One bit inside the ACCESS byte defining the memory protection 0b ... write access is protected by the password verification 1b ... read and write access is protected by the password

Part number	Byte address	Block address	Field	Bit	Default values	description
						verification
FM25NQ04T4	0774h	E4h	CFGLCK	1	0b	Write locking bit for the user configuration excluding the PWD and PACK 0b ... user configuration open to write access 1b ... user configuration permanently locked against write access
FM25NQ04T4	0774h	E4h	NFC_CNT_EN	1	0b	Enables the NFC counter 0b ... disabled 1b ... enabled
FM25NQ04T4	0774h	E4h	NFC_CNT_PWD_PROT_EN	1	0b	enables the password protection to read out and mirror the NFC counter 0b ... the protection is disabled 1b ... the protection is enabled
FM25NQ04T4	0774h	E4h	AUTHLIM	3	000b	Limitation of negative password verification attempts 000b ... limiting of negative password verification attempts disabled 001b-111b ... maximum number of negative password verification attempts
FM25NQ04T4	0777h	DDh	MIRRORS	1	0b	MIRRORS defines the sector address for the beginning of the ASCII mirroring 0b … sector 0 1b … sector1
FM25NQ04T4	0777h	DDh	AUTHS	1	0b	AUTH0 defines the sector address from which the password verification is required. 0b … sector 0 1b … sector1

Remark: The CFGLCK bit activates the permanent write protection of two blocks of configuration. The write lock is only activated after a power cycle of FM25NQ04Tx. If write protection is enabled, each write attempt leads to a NAK response.

Table 22 TAG password and PACK description

Part number	Byte address	Block address	Field	Bit	Default values	description
FM25NQ04T1	00ACh~00AFh	2Bh	PWD	32	all 1b	32-bit password used for memory access protection
FM25NQ04T2	0214h~0217h	85h				
FM25NQ04T3	0394h~0397h	E5h				
FM25NQ04T4	0778h~077Bh	DEh				
FM25NQ04T1	00B0h~00B1h	2Ch	PACK	16	0000h	16-bit password acknowledge used during the password verification process
FM25NQ04T2	0218h~0219h	86h				
FM25NQ04T3	0398h~0399h	E6h				
FM25NQ04T4	077Ch~077Dh	DFh				

7.4 TAG memory status register

TAG memory status register is used to configure the read or write access and the function of GPO, EH_FD pin.

In contact interface, tag status registers can be read using the Read Tag Status Register command. Write access to the Status Register is controlled by the Tag Write Enable command and must be in CT_TAG_PWD authenticated state.

In RF interface, the status register cannot be read or written.

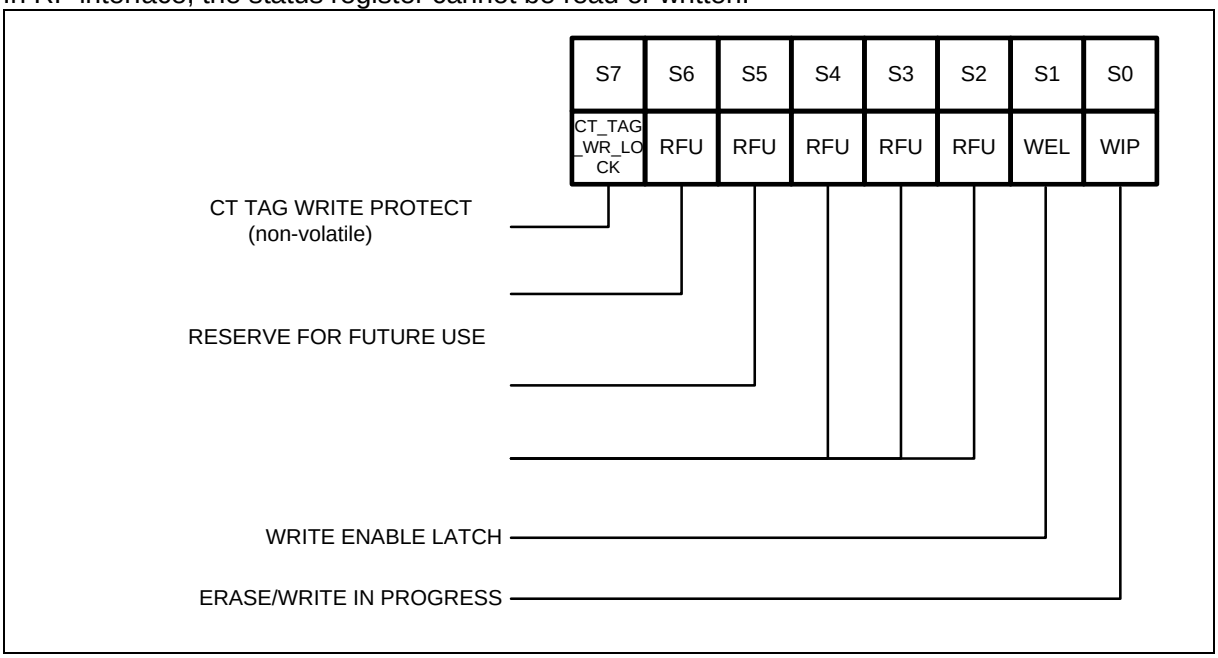


Figure 9 TAG Status Register-1

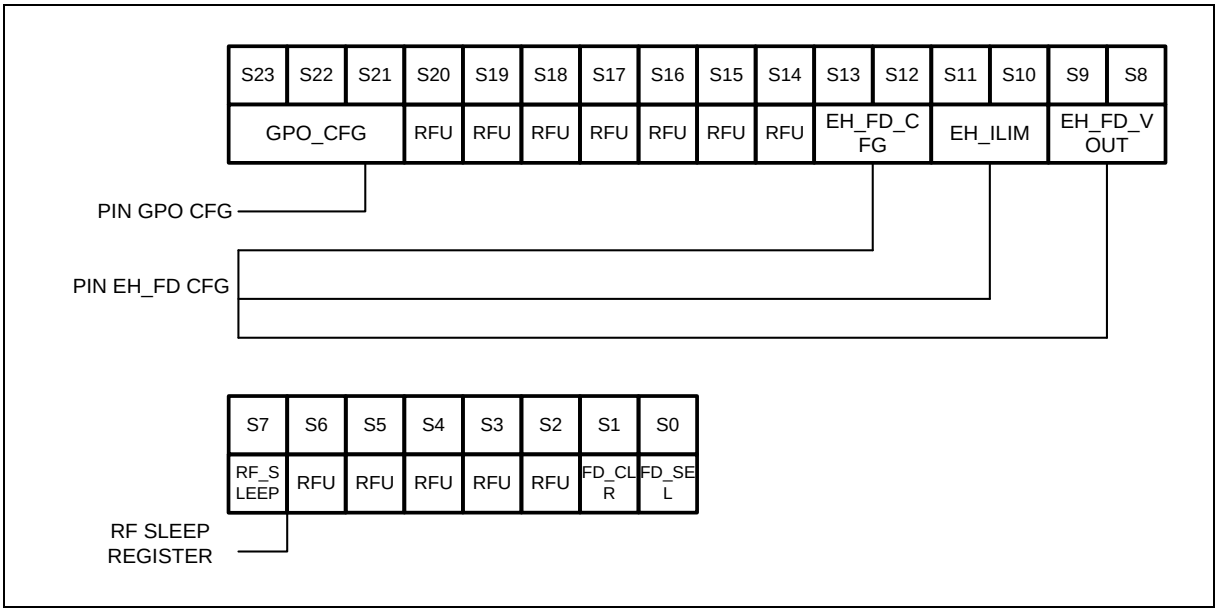


Figure 10 TAG Status Register-2

7.4.1 Contact interface TAG memory write lock bit (CT_TAG_WR_LOCK)

CT_TAG_WR_LOCK is a register that locks the write access of tag memory in contact interface.

In contact interface, the read access of CT_TAG_WR_LOCK doesn't need authentication of CT password (CT_TAG_PWD). However, the write access must be in CT_TAG_PWD authenticated state.

CT_TAG_WR_LOCK does not impact read access of RF interface.

The default value of each bit of CT_TAG_WR_LOCK at delivery is 0b.

7.4.2 TAG WIP Bit

WIP is a read only bit in the status register that is set to a 1 state when the device is executing a Write, Write TAG status register, Write tag password command. During this time the device will ignore further commands to tag memory except for the Read TAG Status Register. When the write command has completed, the WIP bit will be cleared to a 0 state indicating the device is ready for further commands.

7.4.3 TAG Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register that is set to 1 after executing a TAG Write Enable Command. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following commands: Write Disable, Write, Write TAG status register, Write tag password.

7.4.4 GPO PIN Configuration (GPO_CFG)

GPO_CFG is used to configure the function of GPO pin. The default value at delivery is 000b.

- 000b indicates RF access tag busy
- 001b indicates RF access tag WIP
- 010b indicates RF access data busy
- 011b indicates RF access data WIP
- 100b indicates RF in Data memory active status
- 101b indicates FD function
- 110b reserve for future use
- 111b indicates no function

7.4.5 Energy Harvesting and Field Detect Configuration (EH_FD_CFG)

EH_FD_CFG is used to configure the function of EH_FD pin. The default value at delivery is 00b.

- 00b indicates energy harvesting with 100% current drive strength
- 01b indicates energy harvesting with 26% current drive strength
- 10b indicates FD function
- 11b indicates no function (EH_FD pin high Z)

7.4.6 Energy Harvesting Current Limit (EH_ILIM)

EH_ILIM is used to configure the limited current of energy harvesting function. The default value at delivery is 00b.

- 00b indicates no limit.
- 01b indicates I_{LIM}=2mA
- 10b indicates I_{LIM}=1mA
- 11b indicates I_{LIM}=0.5mA

7.4.7 Energy Harvesting and Field Detect Voltage (EH_FD_VOUT)

EH_FD_VOUT is used to configure the output voltage of energy harvesting and FD function. The default value at delivery is 00b.

- 00b indicates Vout=1.8V
- 01b indicates Vout=1.5V
- 10b indicates Vout=2.5V
- 11b indicates Vout=3.3V

7.4.8 RF_SLEEP

RF_SLEEP is used to configure RF sleep function.

- 1b indicates to enable the sleep mode function of RF interface
- 0b indicates to disable the sleep mode function of RF interface
- The default value after power up is 0b

7.4.9 FD_SEL

FD_SEL is used to configure the duration of GPO PIN in FD configuration (GPO_CFG=101b)

- 0b indicates to disable GPO PIN after RF power down
- 1b indicates to disable GPO PIN after FD_CLR set to 1
- The default value after power up is 0b

7.4.10 FD_CLR

FD_CLR is used to disable GPO PIN when FD_SEL is set to 1 and GPO PIN in FD configuration (GPO_CFG=101b)

- 0b indicates to enable GPO PIN
- 1b indicates to disable GPO PIN
- The default value after power up is 0b

8 Contact Interface

FM25NQ04Tx supports the SPI interface access. Any device that sends data to the bus is defined as a transmitter, and any device that reads data is defined as a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which also provides the serial clock for synchronization. FM25NQ04Tx is a slave in all communications.

8.1 SPI operation

8.1.1 Standard SPI

The FM25NQ04Tx is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI commands use the DI input pin to serially write commands, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.

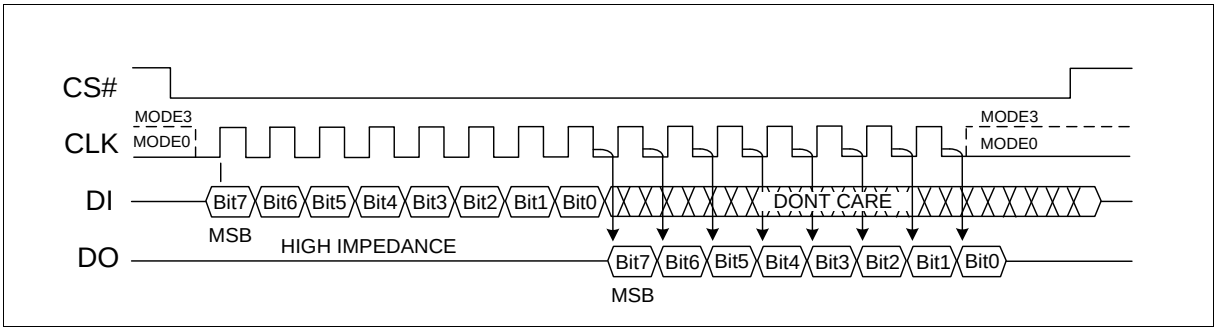


Figure 11 The difference between Mode 0 and Mode 3

8.1.2 Dual SPI

The FM25NQ04TX supports Dual SPI operation when using commands such as “Fast Read Dual Output (3Bh)” and “Fast Read Dual I/O (BBh)”. These commands allow data to be transferred to or from the device at two to three times the rate of ordinary Serial Flash devices. The Dual SPI Read commands are ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed- critical code directly from the SPI bus (XIP). When using Dual SPI commands, the DI and DO pins become bidirectional I/O pins: DQ_0 and DQ_1.

8.1.3 Quad SPI

The FM25NQ04TX supports Quad SPI operation when using commands such as “Fast Read Quad Output (6Bh)”, “Fast Read Quad I/O (EBh)”, “Word Read Quad I/O (E7h)” and “Octal Word Read Quad I/O (E3h)”. These commands allow data to be transferred to or from the device four to six times the rate of ordinary Serial Flash. The Quad Read commands offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI commands the DI and DO pins become bidirectional DQ_0 and DQ_1 and the WP # and HOLD# pins become DQ_2 and DQ_3 respectively. Quad

SPI commands require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

8.1.4 QPI

The FM25NQ04TX supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enable QPI (38h)” command. The typical SPI protocol requires that the byte-long command code being shifted into the device only via DI pin in eight serial clocks. The QPI mode utilizes all four DQ pins to input the command code, thus only two serial clocks are required. This can significantly reduce the SPI command overhead and improve system performance in an XIP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. “Enable QPI (38h)” and “Disable QPI (FFh)” commands are used to switch between these two modes. Upon power-up or after a software reset using “Reset (99h)” command, the default state of the device is Standard/Dual/Quad SPI mode. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI commands, the DI and DO pins become bidirectional DQ_0 and DQ_1, and the WP# and HOLD# pins become DQ_2 and DQ_3 respectively.

8.1.5 Hold

For Standard SPI and Dual SPI operations, the HOLD# signal allows the FM25NQ04TX operation to be paused while it is actively selected (when CS# is low). The HOLD# function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the HOLD# function can save the state of the command and the data in the buffer so programming can resume where it left off once the bus is available again. The HOLD# function is only available for standard SPI and Dual SPI operation, not during Quad SPI or QPI.

To initiate a HOLD# condition, the device must be selected with CS# low. A HOLD# condition will activate on the falling edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will activate after the next falling edge of CLK. The HOLD# condition will terminate on the rising edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will terminate after the next falling edge of CLK. During a HOLD# condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (CS#) signal should be kept active (low) for the full duration of the HOLD# operation to avoid resetting the internal logic state of the device.

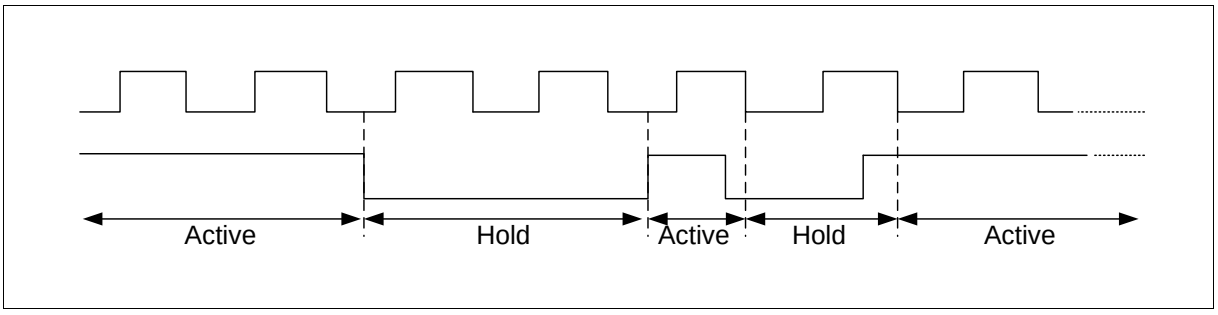


Figure 12 Hold Condition Waveform

8.1.6 Data Operation

FM25NQ04Tx supports data read and write operation of the conventional SPI interface. The detail commands can see 8.4 and 8.5. In addition, the write access of TAG memory can be locked through configuring CT_TAG_WR_LOCK in tag status register, while the write access of DATA memory can be protected by data memory status register, more details refer to 7.2.

8.1.7 Password protection for tag SR and data SR5

To protect TAG status register 1 & 2 and data status register 5 from unexpected write operation,

a password protection mechanism is applied. Before any write operation to these status registers, successful password verification must be applied first. Otherwise the internal write cycle will not be triggered.

Password verification can be enabled using password authentication command. The verification state is effective until power down or a password de-authentication command.

8.2 Field Detection and Energy Harvesting

FM25NQ04Tx features a field detection function. The field detection can be used as interrupt signal. The FD function and the output voltage can be enabled by EH_FD_CFG in TAG Status Register 2 and the trigger condition can be configured by configuration in tag memory.

This pin also features an energy harvesting function. The general purpose of the Energy harvesting is to deliver a part of the non-necessary RF power received by FM25NQ04Tx on the IN1-IN2 RF input in order to supply an external device. The current consumption on EH_FD pin is limited to ensure that the FM25NQ04Tx is correctly supplied during the powering of the external device.

When the Energy harvesting mode is enabled and the power delivered on the IN1-IN2 RF input exceeds the minimum required $P_{IN1\text{-}IN2\_min}$, the FM25NQ04Tx is able to deliver a regulated voltage on EH_FD pin. The output voltage and the drive current can be configured by EH_FD_CFG in TAG Status Register 2. The current consumption on the EH_FD cannot exceed the configured value of IOUT in EH_FD_CFG. Otherwise, the output voltage cannot meet the configured voltage value of EH_FD_CFG.

8.3 GPO Output

FM24NCQ04Tx features a configurable open drain output GPO pin used to provide RF activity or field detection information to an external device. The pin functionality depends on the value of bit[7:5] of GPO_CFG in TAG Status Register 2.

8.3.1 RF data memory Write in progress

When bit[7:5] of GPO_CFG is set to 011b, the pin is configured in RF write data memory in progress mode. The purpose of this mode is to indicate to SPI bus master that some data of data memory has been changed in RF interface.

In this mode, the GPO pin is tied to 0 for the duration of an internal write operation to data memory (i.e. between the end of a valid RF write command and the beginning of the RF answer).

During the execution of SPI write operations, the GPO pin remains in high-Z state.

8.3.2 RF data memory busy

When GPO_CFG is set to 010b, the GPO pin is configured in RF access data memory busy mode. The purpose of this mode is to indicate to SPI bus master whether the data memory of FM24NCQ04Tx is busy in RF interface or not.

In this mode, the GPO pin is tied to 0 from the RF command Start Of Frame (SOF) until the end of the command execution. If a bad RF command is received, the GPO pin is tied to 0 from the RF command SOF until the reception of the RF command CRC. Otherwise, the GPO pin is in high-Z state. When tied to 0, the GPO signal returns to High-Z state if the RF field is cut-off.

During the execution of SPI commands, the GPO pin remains in high-Z state.

8.3.3 RF tag memory Write in progress

When GPO_CFG is set to 001b, the pin is configured in RF write tag memory in progress mode. The purpose of this mode is to indicate to SPI bus master that some data of tag memory has been changed in RF interface.

In this mode, the GPO pin is tied to 0 for the duration of an internal write operation to tag memory (i.e. between the end of a valid RF write command and the beginning of the RF answer).

During the execution of SPI write operations, the GPO pin remains in high-Z state.

8.3.4 RF tag memory busy

When GPO_CFG is set to 000b, the GPO pin is configured in RF access tag memory busy mode. The purpose of this mode is to indicate to SPI bus master whether the tag memory of FM24NCQ04Tx is busy in RF interface or not.

In this mode, the GPO pin is tied to 0 from the RF command Start Of Frame (SOF) until the end of the command execution. If a bad RF command is received, the GPO pin is tied to 0 from the RF command SOF until the reception of the RF command CRC. Otherwise, the GPO pin is in high-Z state. When tied to 0, the GPO signal returns to High-Z state if the RF field is cut-off.

During the execution of SPI commands, the GPO pin remains in high-Z state.

8.3.5 RF Data memory active status

When bit[7:5] of GPO_CFG is set to 100b, the GPO pin is configured in RF data memory active mode. The purpose of this mode is to indicate to the SPI bus master whether the device is in data memory active status.

In this mode, the GPO pin is tied to 0 after receiving Rats command and returns to High-Z state if the RF field is cut-off.

8.3.6 Field detection

When GPO_CFG is set to 101b, the GPO pin is configured in field detect function which can be used as interrupt signal. In this configuration, GPO pin performs the same function as the EH_FD pin in FD configuration, except for GPO pin's open drain feature, while EH_FD features a configurable output voltage. This provides flexible solution for system design.

8.3.7 No function

When GPO_CFG is set to 111b, the GPO pin has no function and remains in high-Z state.

8.4 Data memory Command

The Standard/Dual/Quad SPI command set of the FM25NQ04TX consists of 39 basic commands that are fully controlled through the SPI bus (see Table 24~Table 26 Command Set). Commands are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked into the DI input provides the command code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

The QPI command set of the FM25NQ04TX consists of 25 basic commands that are fully controlled through the SPI bus (see Table 27 Command Set). Commands are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked through DQ[3:0] pins provides the command code. Data on all four DQ pins are sampled on the rising edge of clock with most significant bit (MSB) first. All QPI commands, addresses, data and dummy bytes are using all four DQ pins to transfer every byte of data with every two serial clocks (CLK).

Commands vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Commands are completed with the rising edge of edge CS#. Clock relative timing diagrams for each command are included in Figure 13 through Figure 117. All read commands can be completed after any clocked bit. However, all commands that Write, Program or Erase must complete on a byte boundary (CS# driven high after a full 8-bits have been clocked) otherwise the command will be ignored. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all commands except for Read Status Register will be ignored until the program or erase cycle has completed.

8.4.1 Manufacturer and Device Identification

Table 23 Manufacturer and Device Identification

OP Code	MF7-MF0	ID15-ID0	ID7-ID0
ABh			12h
90h, 92h, 94h	A1h		12h
9Fh	A1h	4013h	

8.4.2 Standard SPI Commands Set

Table 24 Standard SPI Commands Set (1)

COMMAND NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0-7)*	*(8-15)*	*(16-23)*	*(24-31)*	*(32-39)*	*(40-47)*
Write Enable	**06h**					
Volatile SR Write Enable	**50h**					
Write Disable	**04h**					
Read Status Register-1	**05h**	(S7-S0)(2)				
Write Status Register-1	**01h**	S7-S0	01h can be used to program Status Register-1&2			
Read Status Register-2	**35h**	(S15-S8)(2)				
Write Status Register-2	**31h**	S15-S8				
Read Status Register-3	**15h**	(S23-S16)(2)				
Write Status Register-3	**11h**	S23-S16				
Read Status Register-4	**45h**	(S31-S24)(2)				
Write Status Register-4	**41h**	S31-S24				
Read Status Register-5	**8Bh**	S39-S32	S47-S40			
Write Status Register-5	**8Ch**	S39-S32	S47-S40			
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0		
Chip Erase	**C7h/60h**					
Erase / Program Suspend	**75h**					
Erase / Program Resume	**7Ah**					
Power-down	**B9h**					
Read Data	**03h**	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Release Powerdown / ID(4)	**ABh**	dummy	dummy	dummy	(ID7-ID0)(2)	
Manufacturer/Device ID(4)	**90h**	dummy	dummy	00h	(MF7-MF0)	(ID7-ID0)
JEDEC ID(4)	**9Fh**	(MF7-MF0) Manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity		
Read SFDP Register	**5Ah**	00h	00h	A7-A0	dummy	(D7-D0)
Read Unique ID(5)	**4Bh**	dummy	dummy	dummy	dummy	(UID63-UID0)
Erase Security Sectors(6)	**44h**	A23-A16	A15-A8	A7-A0		
Program Security Sectors(6)	**42h**	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0(3)

COMMAND NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Read Security Sectors[6]	**48h**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Individual Sector Lock	**36h**	A23-A16	A15-A8	A7-A0		
Individual Sector Unlock	**39h**	A23-A16	A15-A8	A7-A0		
Read Sector Unlock	**3Dh**	A23-A16	A15-A8	A7-A0		
Global Sector Lock	**7Eh**					
Global Sector Unlock	**98h**					
Enable QPI	**38h**					
Enable Reset	**66h**					
Reset	**99h**					

8.4.3 Dual SPI Commands Set

Table 25 Dual SPI Commands Set

COMMAND NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0-7)*	*(8-15)*	*(16-23)*	*(24-31)*	*(32-39)*	*(40-47)*
Fast Read Dual Output	**3Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, …)[8]
Fast Read Dual I/O	**BBh**	A23-A8[7]	A7-A0, M7-M0 [7]	(D7-D0, …)[8]		
Manufacturer/Device ID by Dual I/O[4]	**92h**	A23-A8[7]	A7-A0, M7-M0[7]	(MF7-MF0, ID7-ID0)		

8.4.4 Quad SPI Commands Set

Table 26 Quad SPI Commands Set

COMMAND NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0-7)*	*(8-15)*	*(16-23)*	*(24-31)*	*(32-39)*	*(40-47)*
Quad Page Program	**32h**	A23-A16	A15-A8	A7-A0	D7-D0, …[10]	D7-D0, …[3]
Fast Read Quad Output	**6Bh**	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, …)[10]
Fast Read Quad I/O	**EBh**	A23-A0, M7-M0[9]	(xxxx, D7-D0)[11]	(D7-D0, …)[10]		
Word Read Quad I/O[13]	**E7h**	A23-A0, M7-M0[9]	(xx, D7-D0)[12]	(D7-D0, …)[10]		
Octal Word Read Quad I/O[14]	**E3h**	A23-A0, M7-M0[9]	(D7-D0, …)[10]			
Set Burst with Wrap	**77h**	xxxxxx, W6-W4[9]				
Manufacture/Device ID by Quad I/O[4]	**94h**	A23-A0, M7-M0[9]	xxxx, (MF7-MF0, ID7-ID0)	(MF7-MF0, ID7-ID0, …)		

8.4.5 QPI Commands Set

Table 27 QPI Commands Set [15]

COMMAND NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
CLOCK NUMBER	*(0,1)*	*(2,3)*	*(4,5)*	*(6,7)*	*(8,9)*	*(10,11)*

COMMAND NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Write Enable	**06h**					
Volatile SR Write Enable	**50h**					
Write Disable	**04h**					
Read Status Register-1	**05h**	(S7-S0)(2)	01h can be used to program Status Register-1&2			
Write Status Register-1	**01h**	S7-S0				
Read Status Register-2	**35h**	(S15-S8)(2)				
Write Status Register-2	**31h**	S18-S8				
Read Status Register-3	**15h**	(S23-S16)(2)				
Write Status Register-3	**11h**	S23-S16				
Page Program	**02h**	A23-A16	A15-A8	A7-A0	D7-D0(10)	D7-D0(3)
Sector Erase (4KB)	**20h**	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	**52h**	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	**D8h**	A23-A16	A15-A8	A7-A0		
Chip Erase	**C7h/60h**					
Erase / Program Suspend	**75h**					
Erase / Program Resume	**7Ah**					
Power-down	**B9h**					
Set Read Parameters	**C0h**	P7-P0				
Fast Read	**0Bh**	A23-A16	A15-A8	A7-A0	dummy(16)	(D7-D0)
Burst Read with Wrap(17)	**0Ch**	A23-A16	A15-A8	A7-A0	dummy(16)	(D7-D0)
Fast Read Quad I/O	**EBh**	A23-A16	A15-A8	A7-A0	M7-M0(16)	(D7-D0)
Release Powerdown / ID(4)	**ABh**	dummy	dummy	dummy	(ID7-ID0)(2)	
Manufacturer/Device ID(4)	**90h**	dummy	dummy	00h	(MF7-MF0)	(ID7-ID0)
JEDEC ID(4)	**9Fh**	(MF7-MF0) Manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity		
Disable QPI	**FFh**					
Enable Reset	**66h**					
Reset	**99h**					

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data output from the device on either 1, 2 or 4 DQ pins.
2. The Status Register contents and Device ID will repeat continuously until CS# terminates the command.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Sectors, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. See Table 23 Manufacturer and Device Identification table for device ID information.
5. This feature is available upon special order. Please contact Shanghai Fudan Microelectronics Group Co., Ltd for details.
6. Security Sector Address:
   Security Sector 1: A23-A16 = 00h; A15-A8 = 10h; A7-A0 = byte address

Security Sector 2: A23-A16 = 00h; A15-A8 = 20h; A7-A0 = byte address
Security Sector 3: A23-A16 = 00h; A15-A8 = 30h; A7-A0 = byte address

7. Dual SPI address input format:
   DQ_0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
   DQ_1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1
8. Dual SPI data output format:
   DQ_0 = (D6, D4, D2, D0)
   DQ_1 = (D7, D5, D3, D1)
9. Quad SPI address input format:
   DQ_0 = A20, A16, A12, A8, A4, A0, M4, M0
   DQ_1 = A21, A17, A13, A9, A5, A1, M5, M1
   DQ_2 = A22, A18, A14, A10, A6, A2, M6, M2
   DQ_3 = A23, A19, A15, A11, A7, A3, M7, M3

   Set Burst with Wrap input format:
   DQ_0 = x, x, x, x, x, x, W4, x
   DQ_1 = x, x, x, x, x, x, W5, x
   DQ_2 = x, x, x, x, x, x, W6, x
   DQ_3 = x, x, x, x, x, x, x, x
10. Quad SPI data input/output format:
    DQ_0 = (D4, D0, …)
    DQ_1 = (D5, D1, …..)
    DQ_2 = (D6, D2, …..)
    DQ_3 = (D7, D3, …..)
11. Fast Read Quad I/O data output format:
    DQ_0 = (x, x, x, x, D4, D0, D4, D0)
    DQ_1 = (x, x, x, x, D5, D1, D5, D1)
    DQ_2 = (x, x, x, x, D6, D2, D6, D2)
    DQ_3 = (x, x, x, x, D7, D3, D7, D3)
12. Word Read Quad I/O data output format:
    DQ_0 = (x, x, D4, D0, D4, D0, D4, D0)
    DQ_1 = (x, x, D5, D1, D5, D1, D5, D1)
    DQ_2 = (x, x, D6, D2, D6, D2, D6, D2)
    DQ_3 = (x, x, D7, D3, D7, D3, D7, D3)
13. For Word Read Quad I/O, the lowest address bit must be 0. (A0 = 0)
14. For Octal Word Read Quad I/O, the lowest four address bits must be 0. (A3, A2, A1, A0 = 0)
15. QPI Command Address, Data input/output format:

CLK#	0	1	2	3	4	5	6	7	8	9	10	11
DQ_0	C4	C0	A20	A16	A12	A8	A4	A0	D4	D0	D4	D0
DQ_1	C5	C1	A21	A17	A13	A9	A5	A1	D5	D1	D5	D1
DQ_2	C6	C2	A22	A18	A14	A10	A6	A2	D6	D2	D6	D2
DQ_3	C7	C3	A23	A19	A15	A11	A7	A3	D7	D3	D7	D3

16. The number of dummy clocks for QPI Fast Read, QPI Fast Read Quad I/O & QPI Burst Read with Wrap is controlled by read parameter P7 ~ P4.
17. The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P3 ~ P0.

8.4.6 Write Enable (WREN) (06h)

The Write Enable (WREN) command (Figure 13) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Sectors command. The Write Enable **(**WREN**)** command is entered by driving CS# low, shifting the command code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

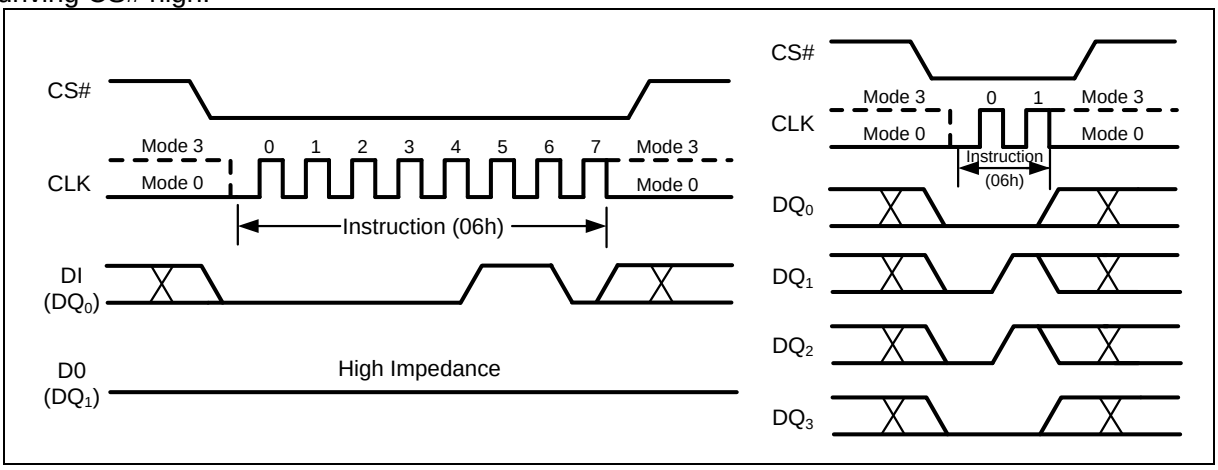


Figure 13 Write Enable Command for SPI Mode (left) or QPI Mode (right)

8.4.7 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 10.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) command must be issued prior to a Write Status Register (01h/31h/11h) command. Write Enable for Volatile Status Register command (Figure 14) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

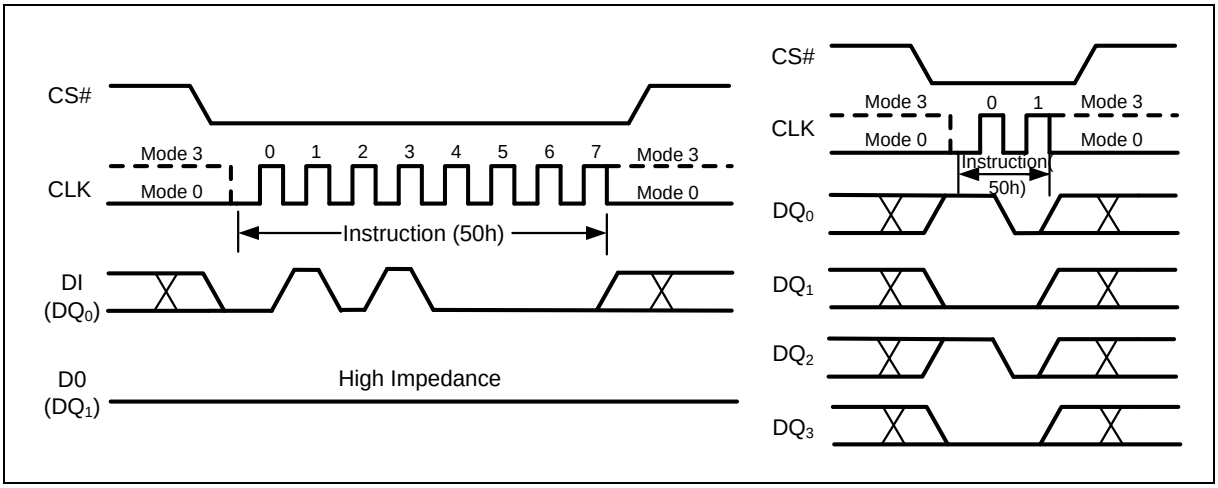


Figure 14 Write Enable for Volatile Status Register Command for SPI Mode (left) or QPI Mode (right)

8.4.8 Write Disable (WRDI) (04h)

The Write Disable (WRDI) command (Figure 15) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable (WRDI) command is entered by driving CS# low, shifting the command code “04h” into the DI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Sectors, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase and Reset commands.

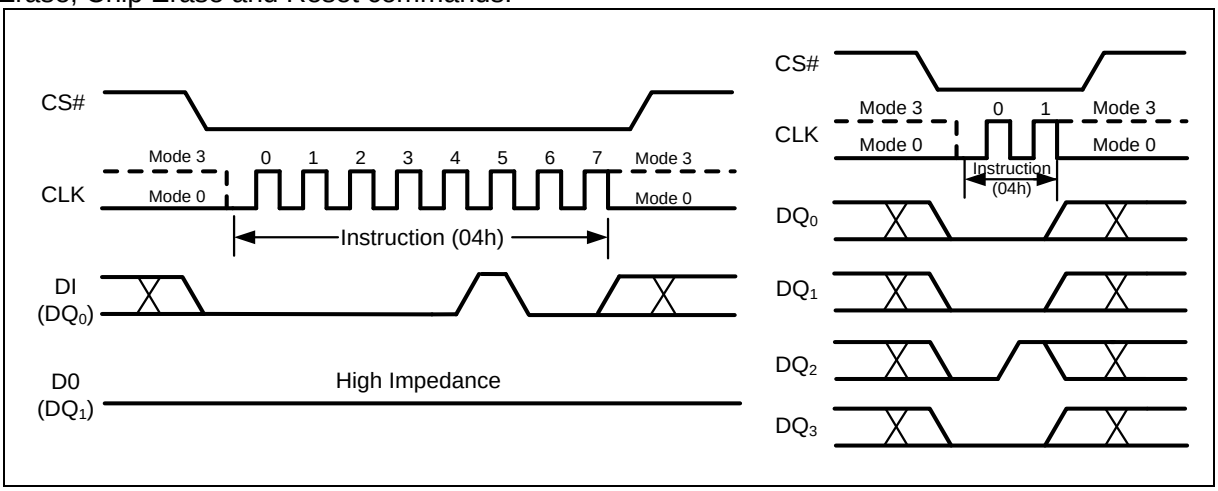


Figure 15 Write Disable Command for SPI Mode (left) or QPI Mode (right)

8.4.9 Read Status Register-1 (RDSR1) (05h) , Status Register-2 (RDSR2) (35h) & Status Register-3 (RDSR3) (15h) & Status Register-4 (RDSR4) (45h)

The Read Status Register commands allow the 8-bit Status Registers to be read. The command is entered by driving CS# low and shifting the command code “05h” for Status Register-1, “35h” for Status Register-2 or “15h” for Status Register-3 or “45h” for Status Register-4 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 16. The Status Register bits are shown in Figure 2 , Figure 3，Figure 4 and Figure 5.

The Read Status Register command may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the WIP status bit to be checked to determine when the cycle is complete and if the device can accept another command. The Status Register can be read continuously, as shown in Figure 17. The command is completed by driving CS# high.

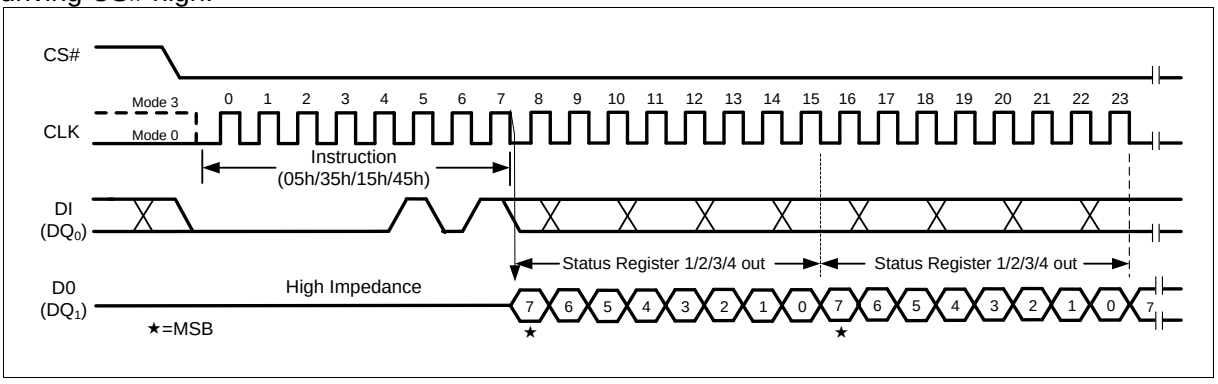


Figure 16 Read Status Register Command (SPI Mode)

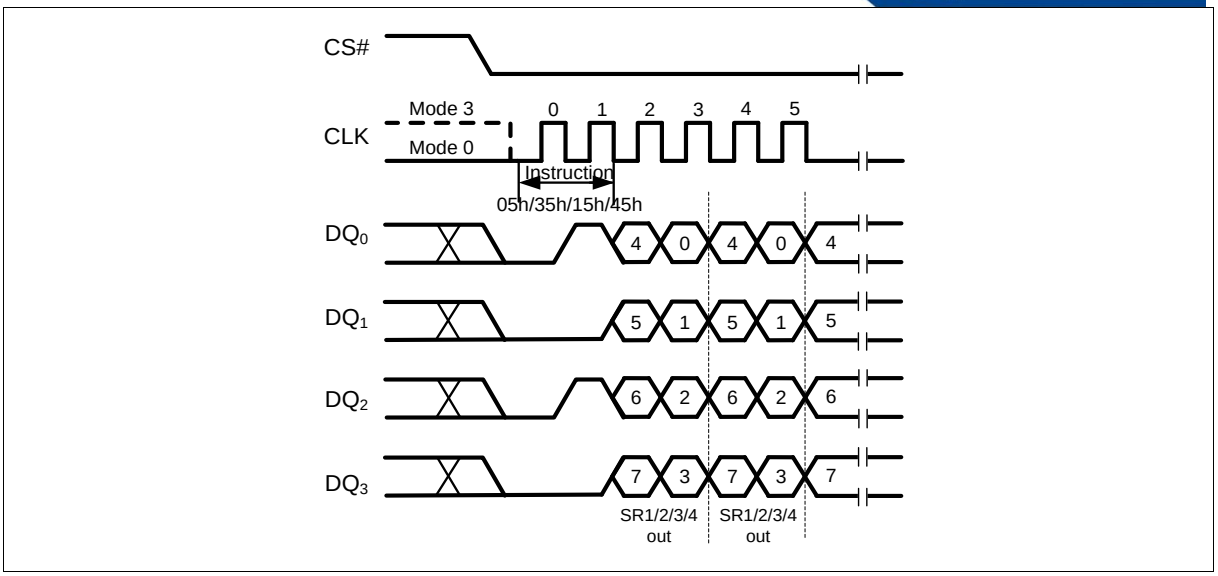


Figure 17 Read Status Register Command (QPI Mode)

8.4.10 Write Status Register-1(WRSR) (01h), Status Register-2 (31h) & Status Register-3 (11h) & Status Register-4 (41h)

The Write Status Register (WRSR) command allows the Status Register to be written. Only non-volatile Status Register bits SRP0, SEC, TB, BP2, BP1, BP0 (bits 7 thru 2 of Status Register-1) , CMP, LB1, LB0 QE, SRP1 (bits 12 thru 8 of Status Register-2) , WPS, DRV0, DRV1(bits 2 thru 0 of Status Register-3) and PTB, PD6-PD0(Status Register-4) can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register (WRSR) command. LB1-0 are non-volatile OTP bits, once it is set to 1, it cannot be cleared to 0. The Status Register bits are shown in shown in Figure 2 , Figure 3 ,Figure 4 and Figure 5 and described in 7.2 Data memory status register.

To write non-volatile Status Register bits, a standard Write Enable (06h) command must previously have been executed for the device to accept the Write Status Register (WRSR) command (Status Register bit WEL must equal 1). Once write enabled, the command is entered by driving CS# low, sending the command code “01h”, and then writing the status register data byte as illustrated in Figure 18 and Figure 19.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) command must have been executed prior to the Write Status Register (WRSR) command (Status Register bit WEL remains 0). However, SRP1 and LB1-0, cannot be changed from “1” to “0” because of the OTP protection for these bits. Upon power off or the execution of a “Reset (99h)” command, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be restored.

To complete the Write Status Register (WRSR) command, the CS# pin must be driven high after the eighth or sixteenth bit of data that is clocked in. If this is not done the Write Status Register (WRSR) command will not be executed. If CS# is driven high after the eighth clock the CMP, QE and SRP1 bits will be cleared to 0.

During non-volatile Status Register write operation (06h combined with 01h), after CS# is driven high, the self-timed Write Status Register cycle will commence for a time duration of t_W (See “11.2.3_AC Characteristics”). While the Write Status Register cycle is in progress, the Read Status Register command may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other commands again. After the Write Status Register cycle has finished, the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

During volatile Status Register write operation (50h combined with 01h), after CS# is driven high, the Status Register bits will be refreshed to the new values within the time period of t_{SHSL2} (See "11.2.3 AC Characteristics"). WIP bit will remain 0 during the Status Register bit refresh period.

The Write Status Register (WRSR) command can be used in both SPI mode and QPI mode. However, the QE bit cannot be written to when the device is in the QPI mode, because QE=1 is required for the device to enter and operate in the QPI mode.

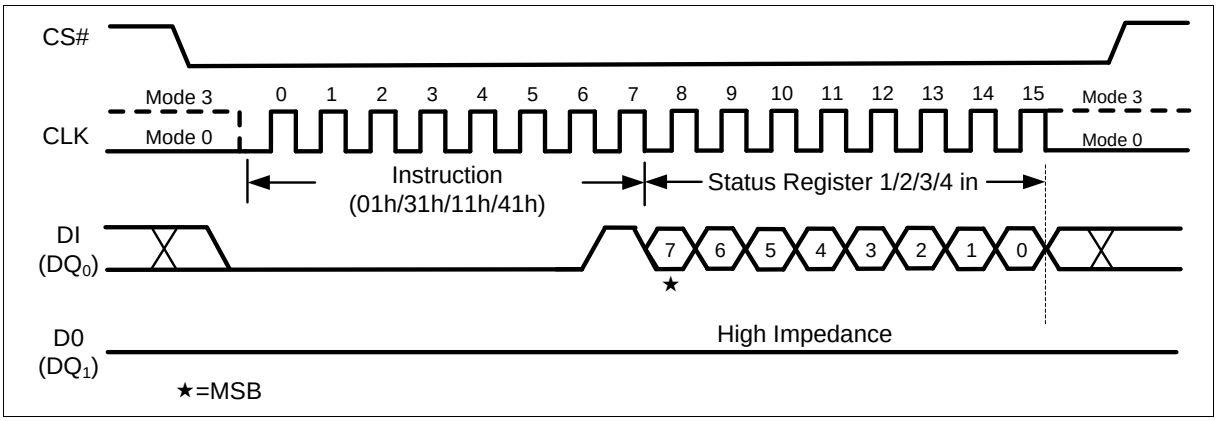


Figure 18 Write Status Register Command (SPI Mode)

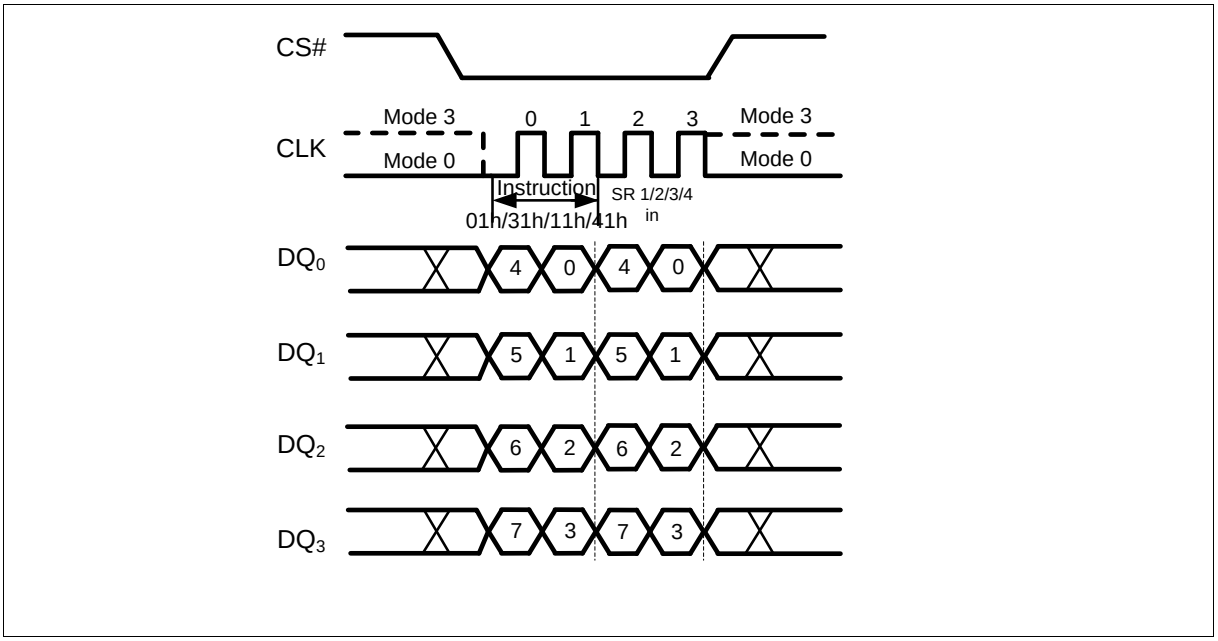


Figure 19 Write Status Register Command (QPI Mode)

The FM25NQ04TX is also backward compatible to FMSH's previous generations of serial flash memories, in which the Status Register-1&2 can be written using a single "Write Register-1(01h)" command. To complete the Write Status Register1&2, the CS# pin must be driven high after the sixteenth bit of data that is clocked in as shown in Figure 20 & Figure 21 . If CS# is driven high after the eighth clock, the Write Status Register (WRSR) command will only program the Status Register-1, the Status Register-2 will not be affected.

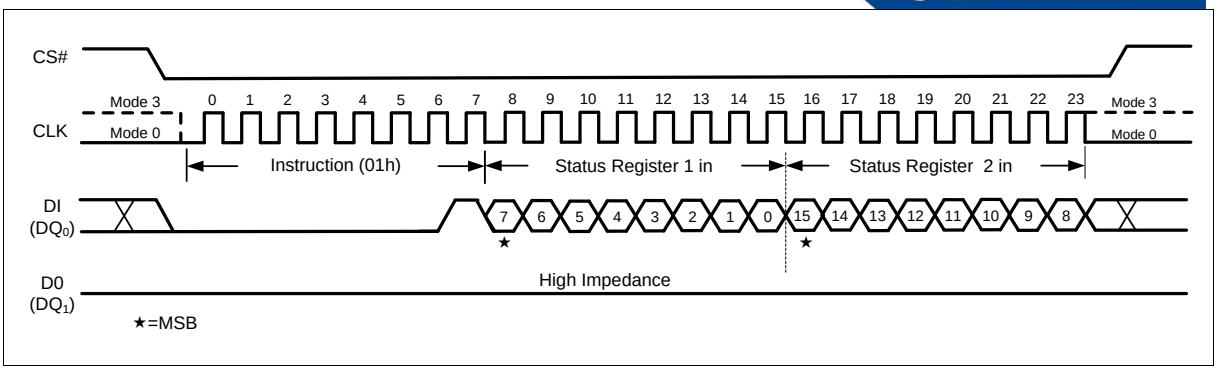


Figure 20 Write Status Register-1/2 Command (backward compatible, SPI Mode)

错误！不能通过编辑域代码创建对象。

Figure 21 Write Status Register-1/2 Command (backward compatible, QPI Mode)

8.4.11 Read Data (03h)

The Read Data command allows one or more data bytes to be sequentially read from the memory. The command is initiated by driving the CS# pin low and then shifting the command code “03h” followed by a 24-bit address A23-A0 into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single command as long as the clock continues. The command is completed by driving CS# high.

The Read Data command sequence is shown in Figure 22. If a Read Data command is issued while an Erase, Program or Write cycle is in process (WIP =1) the command is ignored and will not have any effect on the current cycle. The Read Data command allows clock rates from D.C. to a maximum of f_R (see “11.2.3_AC Characteristics”).

The Read Data (03h) command is only supported in Standard SPI mode.

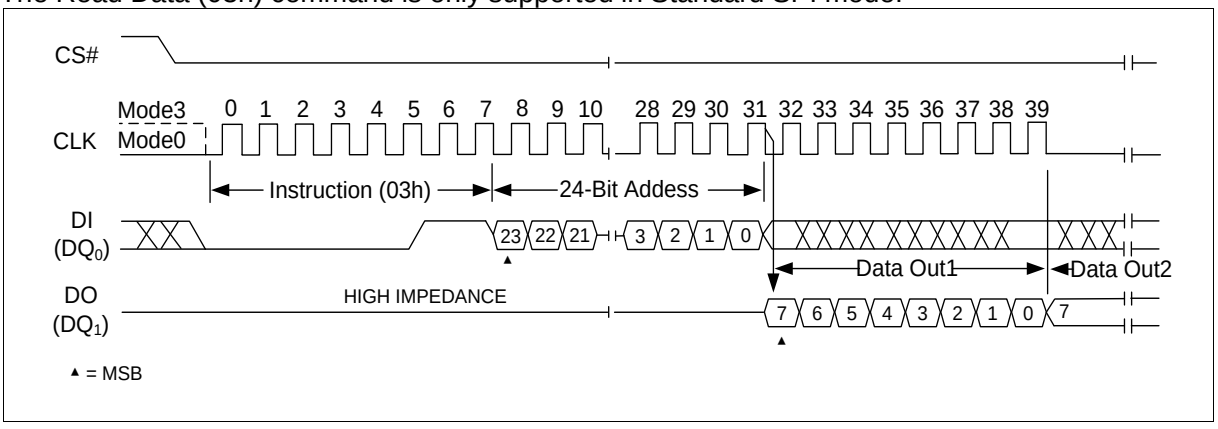


Figure 22 Read Data Command (SPI Mode only)

8.4.12 Fast Read (0Bh)

The Fast Read command is similar to the Read Data command except that it can operate at the highest possible frequency of F_R (see “11.2.3_AC Characteristics”). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 23. The dummy clocks

allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DI pin is a “don’t care”.

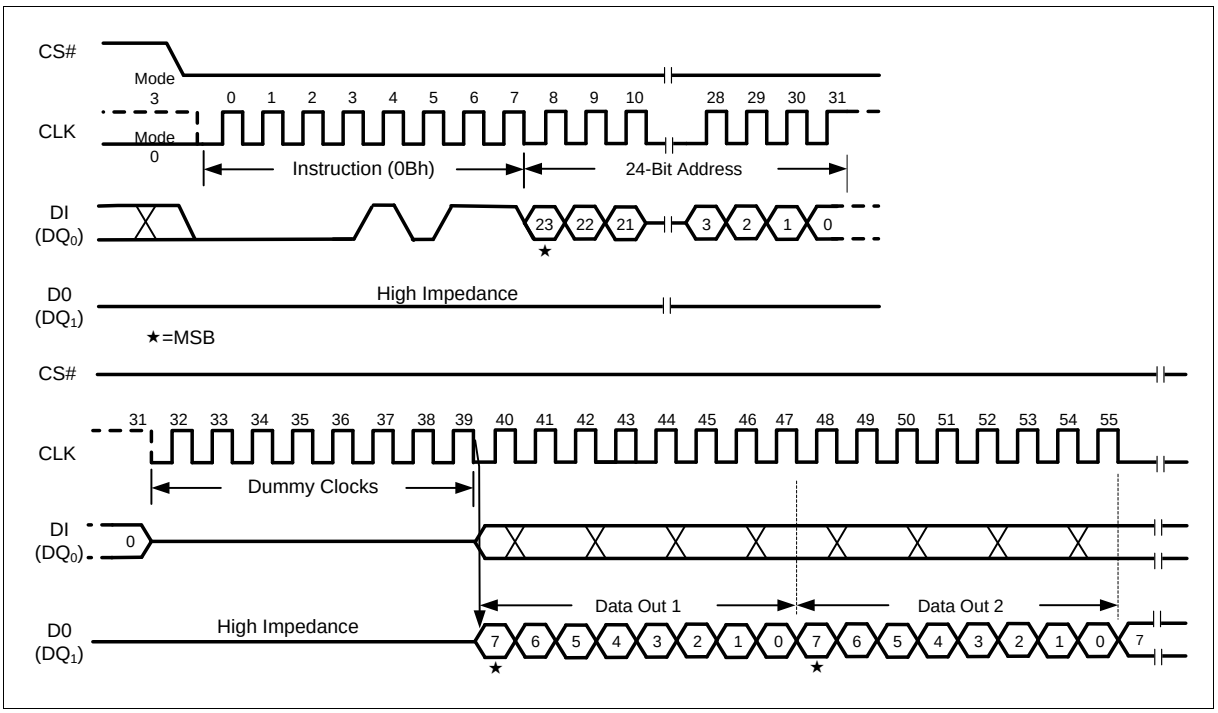


Figure 23 Fast Read Command (SPI Mode)

Fast Read (0Bh) in QPI Mode

The Fast Read command is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” command to accommodate wide range applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 2, 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset command is 2.

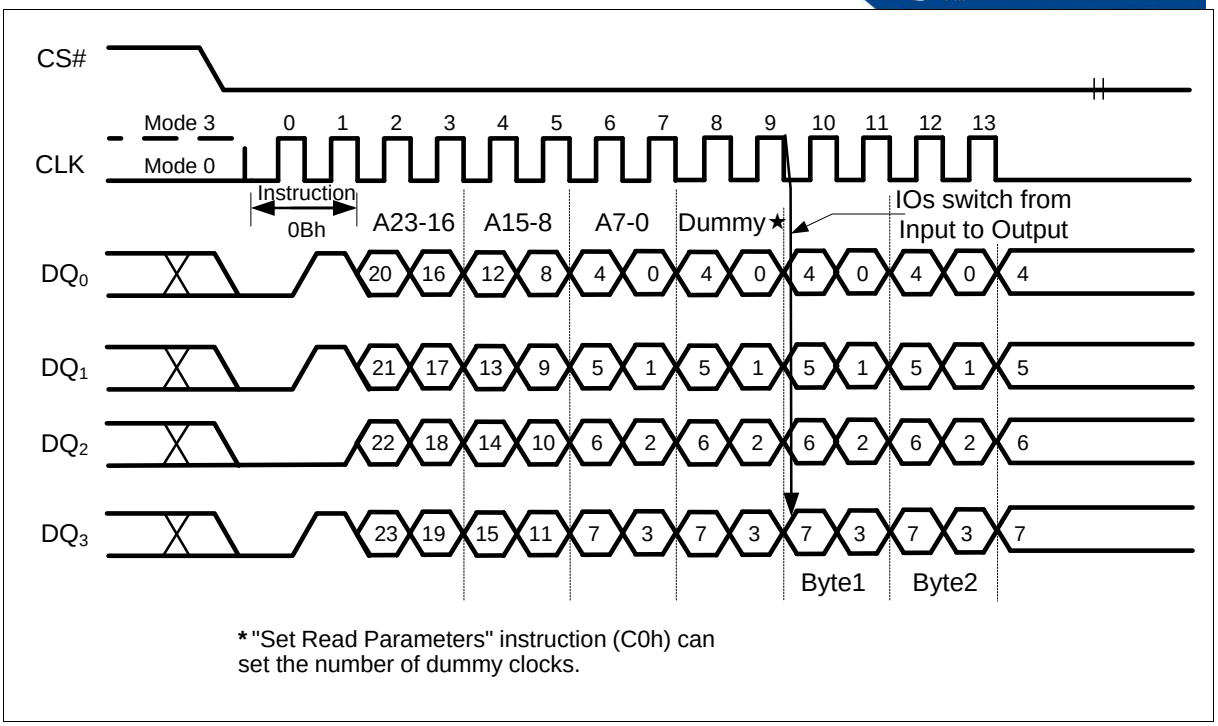


Figure 24 Fast Read Command (QPI Mode)

8.4.13 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) command is similar to the standard Fast Read (0Bh) command except that data is output on two pins; DQ_0 and DQ_1. This allows data to be transferred from the FM25NQ04TX at twice the rate of standard SPI devices. The Fast Read Dual Output command is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read command, the Fast Read Dual Output command can operate at the highest possible frequency of F_R (see “11.2.3_AC Characteristics”). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 25. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the DQ_0 pin should be high-impedance prior to the falling edge of the first data out clock.

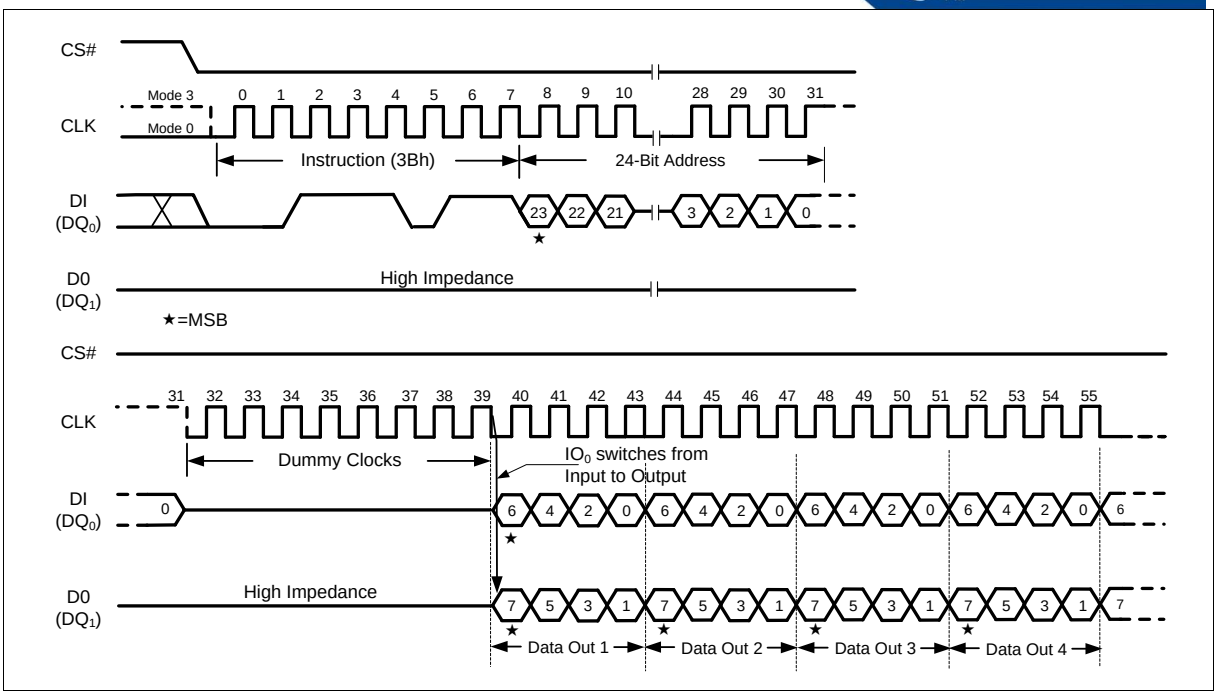


Figure 25 Fast Read Dual Output Command (SPI Mode only)

8.4.14 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) command is similar to the Fast Read Dual Output (3Bh) command except that data is output on four pins, DQ_0, DQ_1, DQ_2, and DQ_3. A Quad enable of Status Register-2 must be executed before the device will accept the Fast Read Quad Output Command (Status Register bit QE must equal 1). The Fast Read Quad Output Command allows data to be transferred from the FM25NQ04TX at four times the rate of standard SPI devices.

The Fast Read Quad Output command can operate at the highest possible frequency of F_R (see “11.2.3_AC Characteristics”). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 26. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

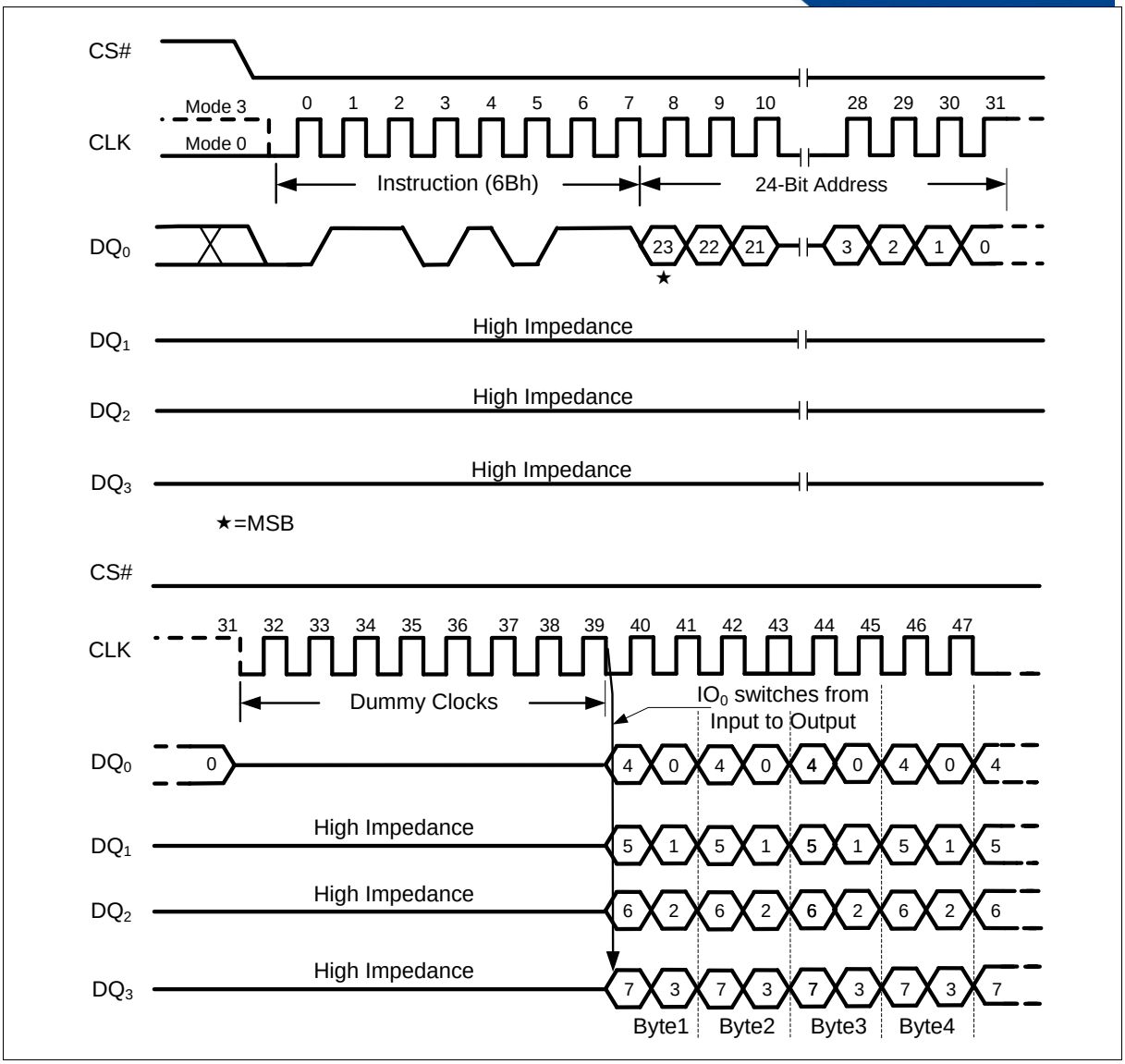


Figure 26 Fast Read Quad Output Command (SPI Mode only)

8.4.15 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) command allows for improved random access while maintaining two I/O pins, DQ_0 and DQ_1. It is similar to the Fast Read Dual Output (3Bh) command but with the capability to input the Address bits A23-A0 two bits per clock. This reduced command overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Fast Read Dual I/O with "Continuous Read Mode"

The Fast Read Dual I/O command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits A23-A0, as shown in Figure 27. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O command through the inclusion or exclusion of the first byte command code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O command (after CS# is raised and then lowered) does not require the BBh command code, as shown in Figure 28. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do

not equal to (1,0), the next command (after CS# is raised and then lowered) requires the first byte command code, thus returning to normal operation. It is recommended to input FFFFh on DQ_0 for the next

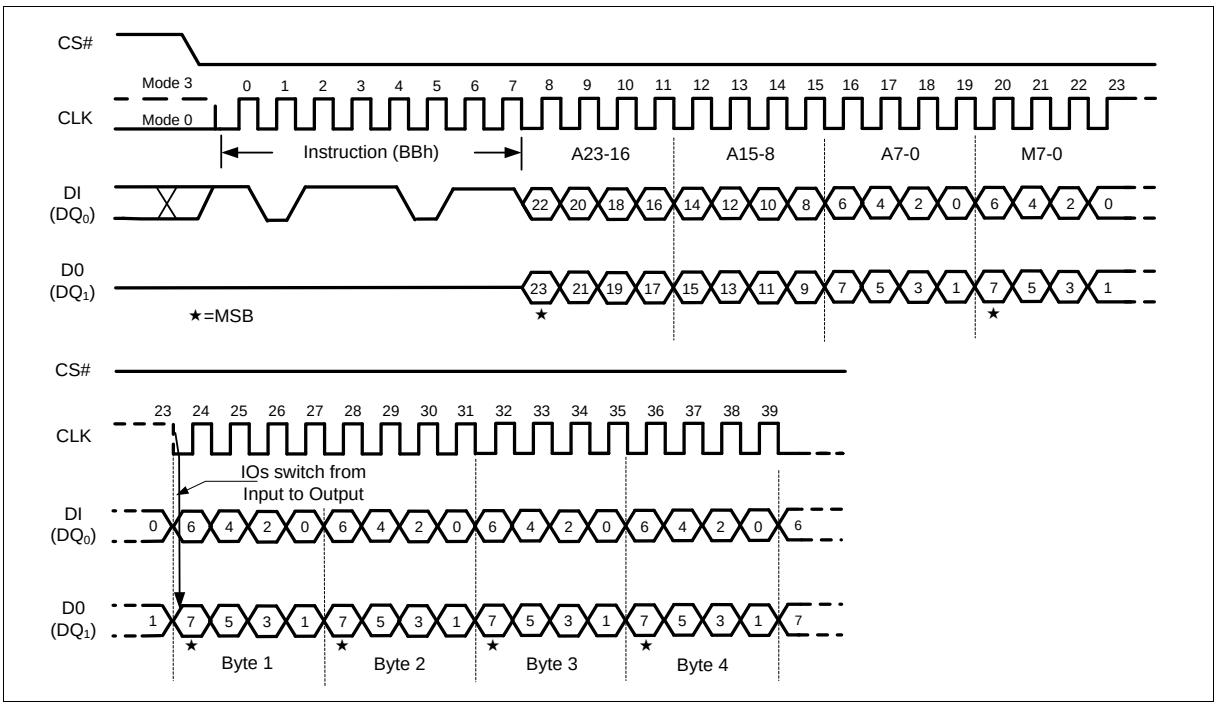


Figure 27 Fast Read Dual I/O Command (Initial command or previous M5-4 ≠ 10, SPI Mode only)

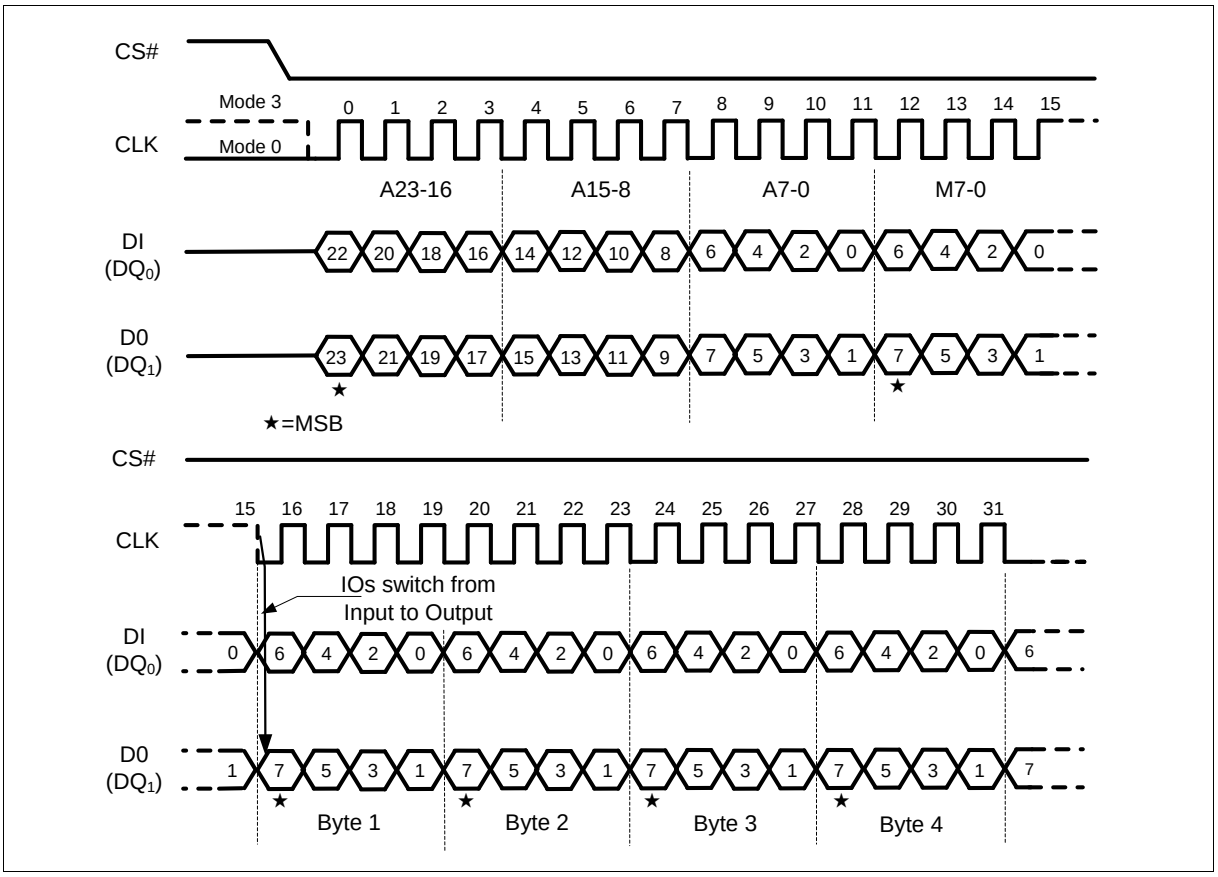


Figure 28 Fast Read Dual I/O Command (Previous command set M5-4 = 10, SPI Mode only)

8.4.16 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) command is similar to the Fast Read Dual I/O (BBh) command except that address and data bits are input and output through four pins DQ_0, DQ_1, DQ_2 and DQ_3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces command overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Command.

Fast Read Quad I/O with "Continuous Read Mode"

The Fast Read Quad I/O command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits A23-A0, as shown in Figure 29. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O command through the inclusion or exclusion of the first byte command code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O command (after CS# is raised and then lowered) does not require the EBh command code, as shown in Figure 30. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next command (after CS# is raised and then lowered) requires the first byte command code, thus returning to normal operation. It is recommended to input FFh on DQ_0 for the next command (8 clocks), to ensure M4 = 1 and return the device to normal operation.

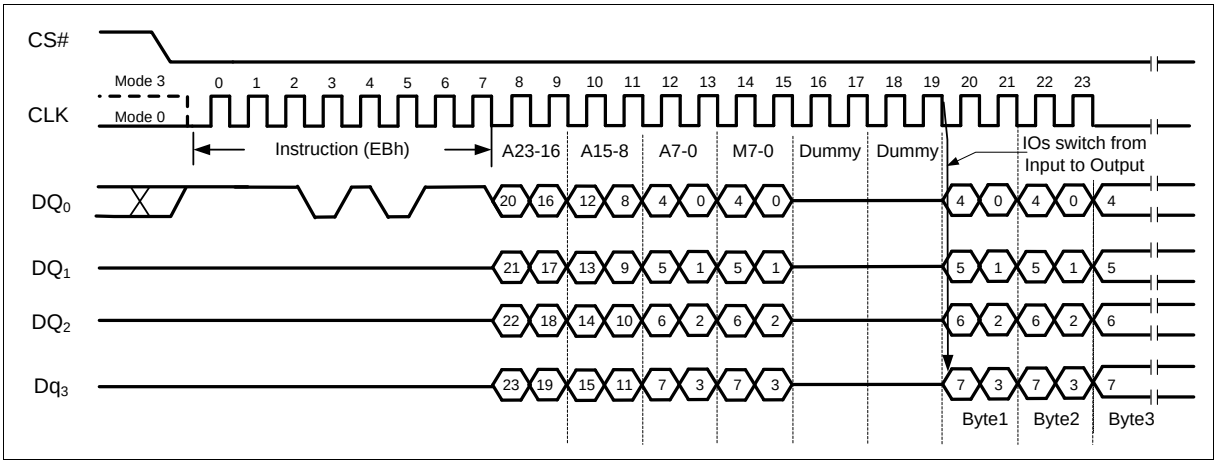


Figure 29 Fast Read Quad I/O Command (Initial command or previous M5-4≠10, SPI Mode)

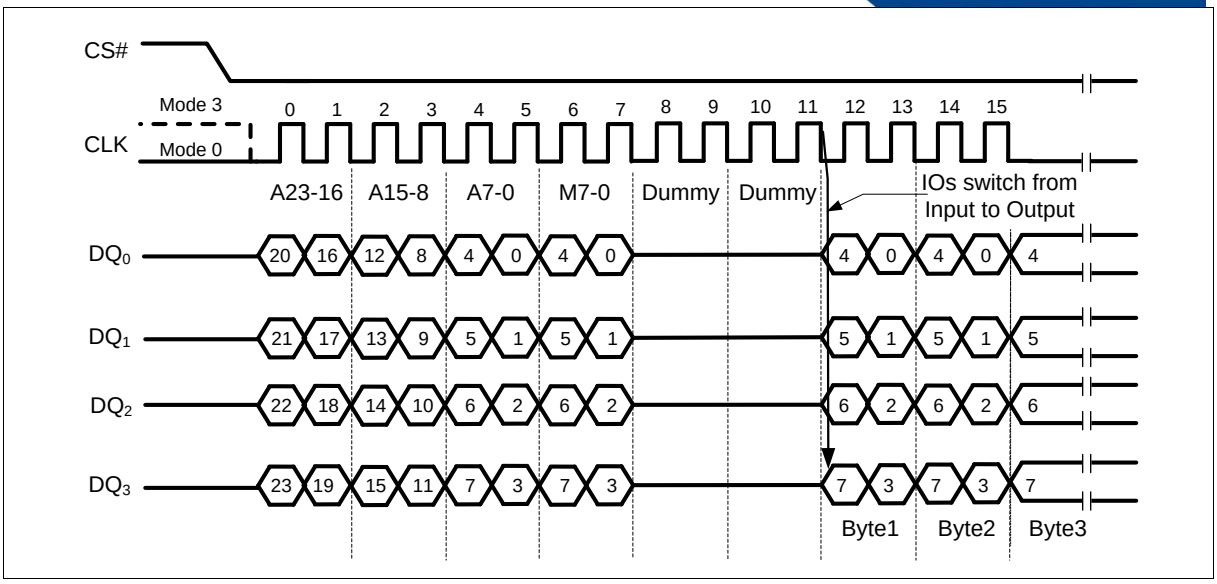


Figure 30 Fast Read Quad I/O Command (Previous command set M5-4 = 10, SPI Mode)

Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O command can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to EBh. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following EBh commands. When "Wrap Around" is enabled, the data being accessed can be limited to either a 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" command allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See "8.4.19 Set Burst with Wrap (77h)" for detail descriptions.

Fast Read Quad I/O (EBh) in QPI Mode

The Fast Read Quad I/O command is also supported in QPI mode, as shown in Figure 31. When QPI mode is enabled, the number of dummy clocks is configured by the "Set Read Parameters (C0h)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 2, 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset command is 2. In QPI mode, the "Continuous Read Mode" bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Continuous Read Mode bits immediately.

"Continuous Read Mode" feature is also available in QPI mode for Fast Read Quad I/O command. Please refer to the description on previous pages.

"Wrap Around" feature is not available in QPI mode for Fast Read Quad I/O command. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0Ch) command must be used. Please refer to "8.4.40 Burst Read with Wrap (0Ch)" for details.

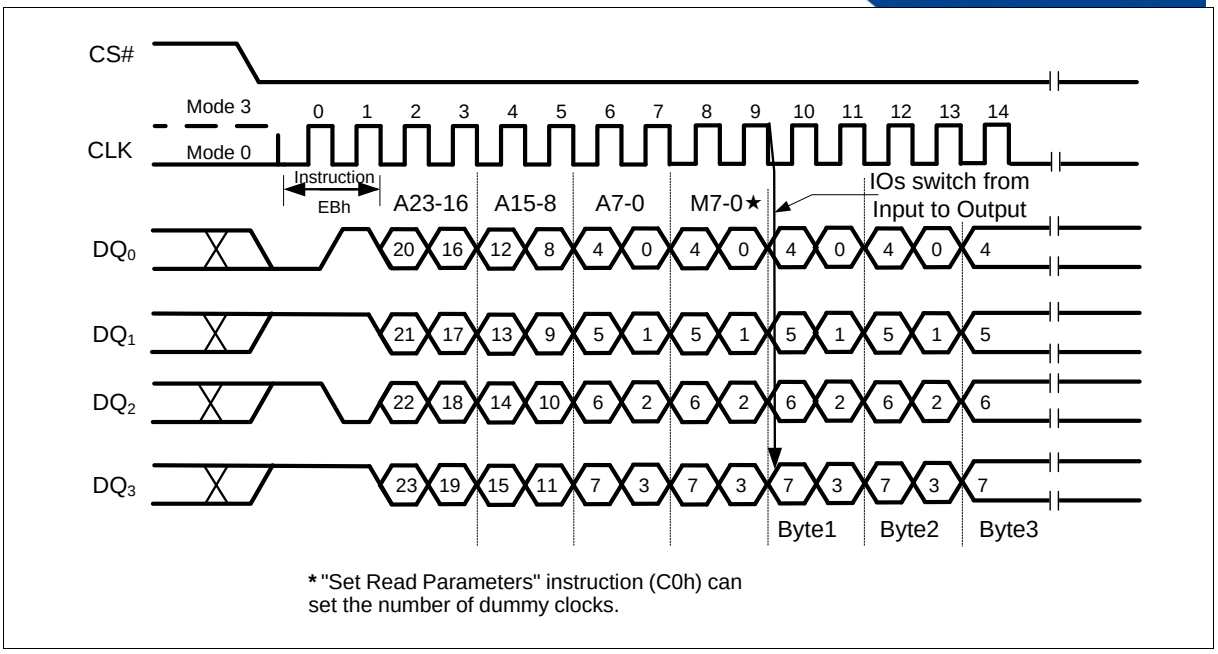


Figure 31 Fast Read Quad I/O Command (Initial command or previous M5-4≠10, QPI Mode)

8.4.17 Word Read Quad I/O (E7h)

The Word Read Quad I/O (E7h) command is similar to the Fast Read Quad I/O (EBh) command except that the lowest Address bit (A0) must equal 0 and only two Dummy clock are required prior to the data output. The Quad I/O dramatically reduces command overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Word Read Quad I/O Command.

Word Read Quad I/O with "Continuous Read Mode"

The Word Read Quad I/O command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits A23-A0, as shown in Figure 32. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O command through the inclusion or exclusion of the first byte command code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O command (after CS# is raised and then lowered) does not require the E7h command code, as shown in Figure 33. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next command (after CS# is raised and then lowered) requires the first byte command code, thus returning to normal operation. It is recommended to input FFh on DQ_0 for the next command (8 clocks), to ensure M4 = 1 and return the device to normal operation.

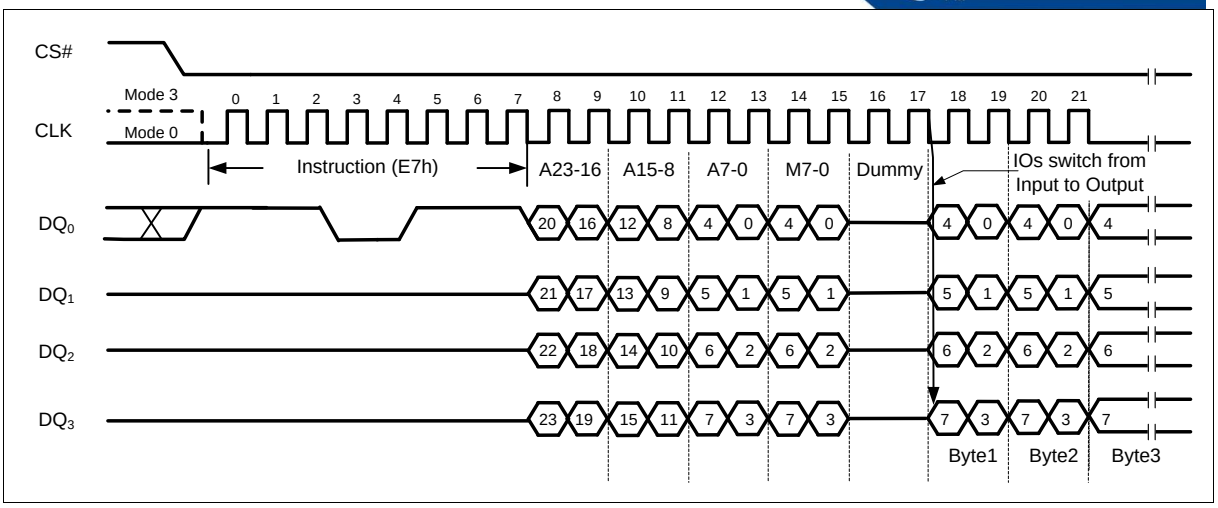


Figure 32 Word Read Quad I/O Command (Initial command or previous M5-4 ≠ 10, SPI Mode only)

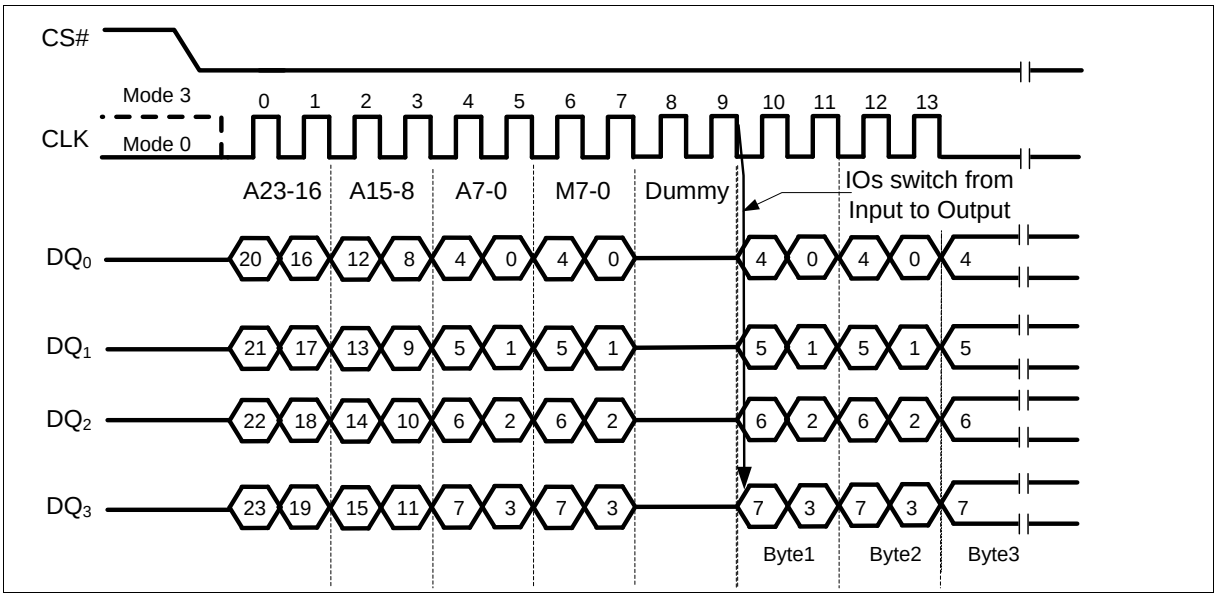


Figure 33 Word Read Quad I/O Command (Previous command set M5-4 = 10, SPI Mode only)

Word Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Word Read Quad I/O command can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to E7h. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following E7h commands. When "Wrap Around" is enabled, the data being accessed can be limited to either a 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" command allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. See "8.4.19 Set Burst with Wrap (77h)" for detail descriptions.

8.4.18 Octal Word Read Quad I/O (E3h)

The Octal Word Read Quad I/O (E3h) command is similar to the Fast Read Quad I/O (EBh) command except that the lower four Address bits (A0, A1, A2, A3) must equal 0. As a result, the dummy clocks are not required, which further reduces the command overhead allowing even faster random access for code execution (XIP). The Quad Enable bit (QE) of Status Register-2 must be set to enable the Octal Word Read Quad I/O Command.

Octal Word Read Quad I/O with "Continuous Read Mode"

The Octal Word Read Quad I/O command can further reduce command overhead through setting the "Continuous Read Mode" bits M7-M0 after the input Address bits A23-A0, as shown in Figure 34. The upper nibble of the (M7-4) controls the length of the next Octal Word Read Quad I/O command through the inclusion or exclusion of the first byte command code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the DQ pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O command (after CS# is raised and then lowered) does not require the E3h command code, as shown in Figure 35. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1, 0), the next command (after CS# is raised and then lowered) requires the first byte command code, thus returning to normal operation. It is recommended to input FFh on DQ_0 for the next command (8 clocks), to ensure M4 = 1 and return the device to normal operation.

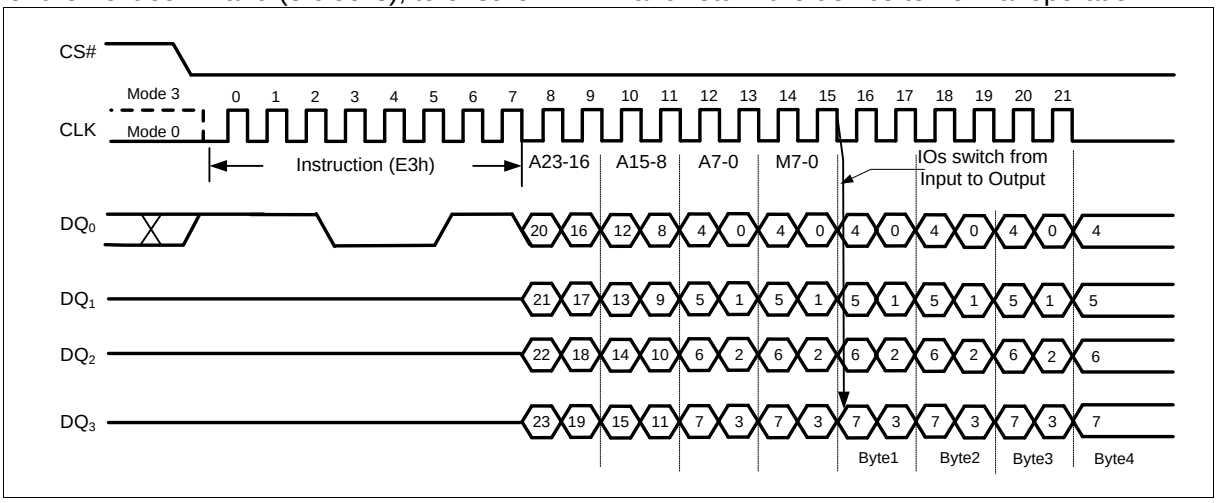


Figure 34 Octal Word Read Quad I/O Command (Initial command or previous M5-4 ≠ 10, SPI Mode only)

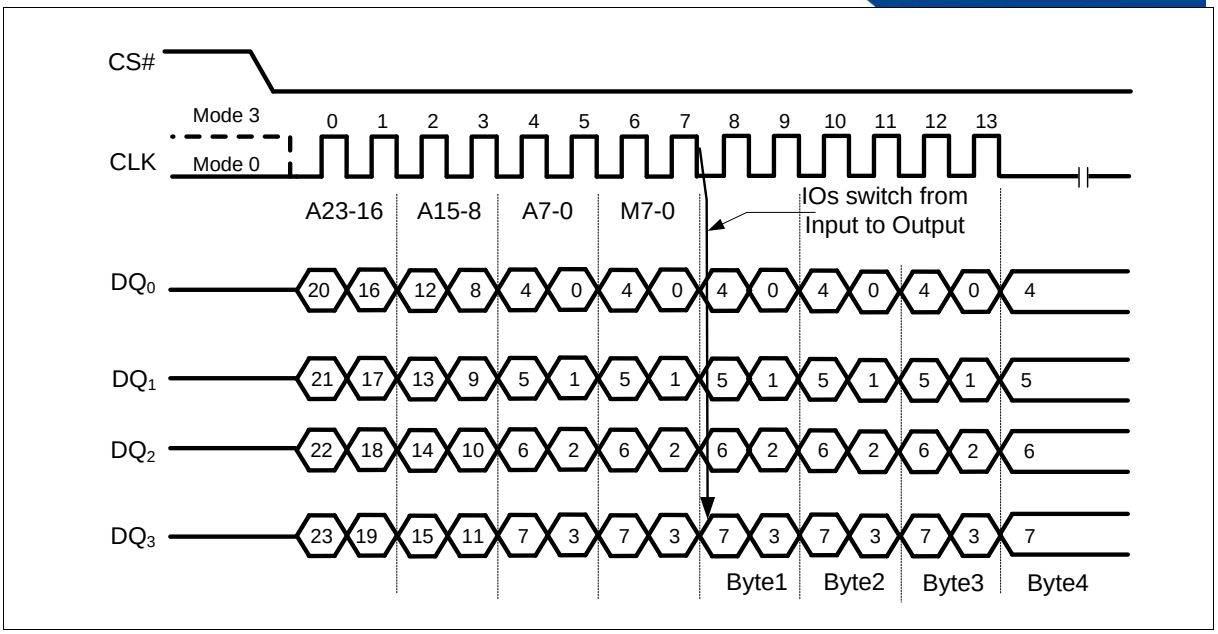


Figure 35 Octal Word Read Quad I/O Command (Previous command set M5-4 = 10, SPI Mode only)

8.4.19 Set Burst with Wrap (77h)

In Standard SPI mode, the Set Burst with Wrap (77h) command is used in conjunction with “Fast Read Quad I/O” and “Word Read Quad I/O” commands to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O command, the Set Burst with Wrap command is initiated by driving the CS# pin low and then shifting the command code “77h” followed by 24 dummy bits and 8 “Wrap Bits”, W7-0. The command sequence is shown in Figure 36. Wrap bit W7 and the lower nibble W3-0 are not used.

W6, W5	W4 = 0		W4 =1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap command, all the following “Fast Read Quad I/O” and “Word Read Quad I/O” commands will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4 = 1. The default value of W4 upon power on is 1. In the case of a system Reset while W4 = 0, it is recommended that the controller issues a Set Burst with Wrap command to reset W4 = 1 prior to any normal Read commands since FM25NQ04TX does not have a hardware Reset Pin.

In QPI mode, the “Burst Read with Wrap (0Ch)” command should be used to perform the Read operation with “Wrap Around” feature. The Wrap Length set by W5-4 in Standard SPI mode is still valid in QPI mode and can also be re-configured by “Set Read Parameters (C0h)” command. Refer to “8.4.39 Set Read Parameters (C0h)” and “8.4.40 Burst Read with Wrap (0Ch)” for details.

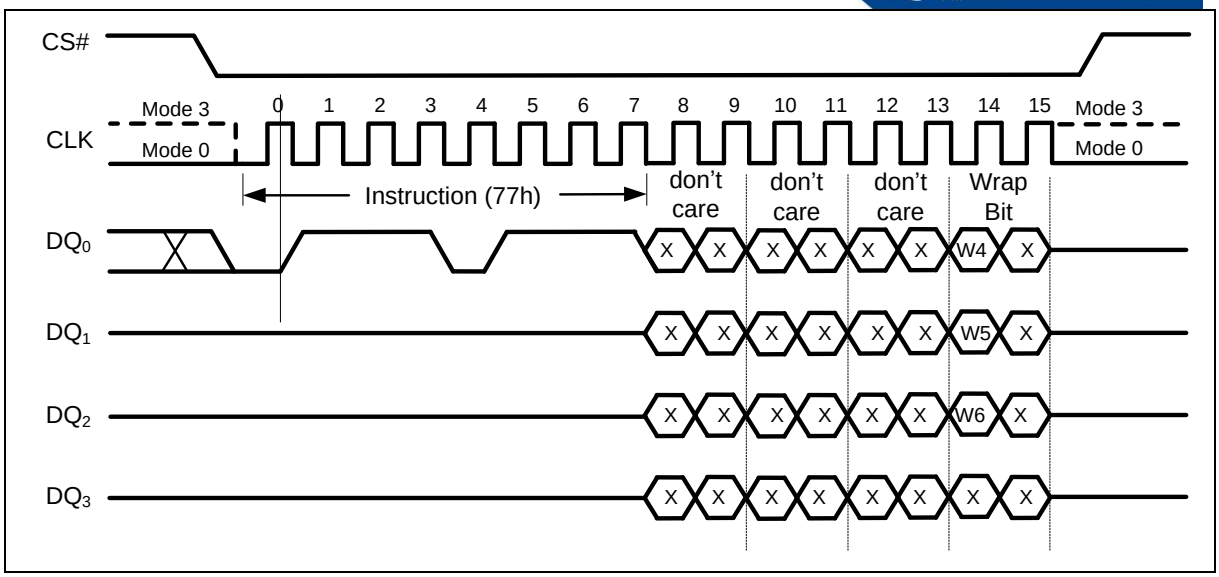


Figure 36 Set Burst with Wrap Command (SPI Mode only)

8.4.20 Page Program (02h)

The Page Program command allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable command must be executed before the device will accept the Page Program Command (Status Register bit WEL= 1). The command is initiated by driving the CS# pin low then shifting the command code "02h" followed by a 24-bit address A23-A0 and at least one data byte, into the DI pin. The CS# pin must be held low for the entire length of the command while data is being sent to the device. The Page Program command sequence is shown in Figure 37 and Figure 38.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase commands, the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program command will not be executed. After CS# is driven high, the self-timed Page Program command will commence for a time duration of t_{PP} (See "11.2.3 AC Characteristics"). While the Page Program cycle is in progress, the Read Status Register command may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program command will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

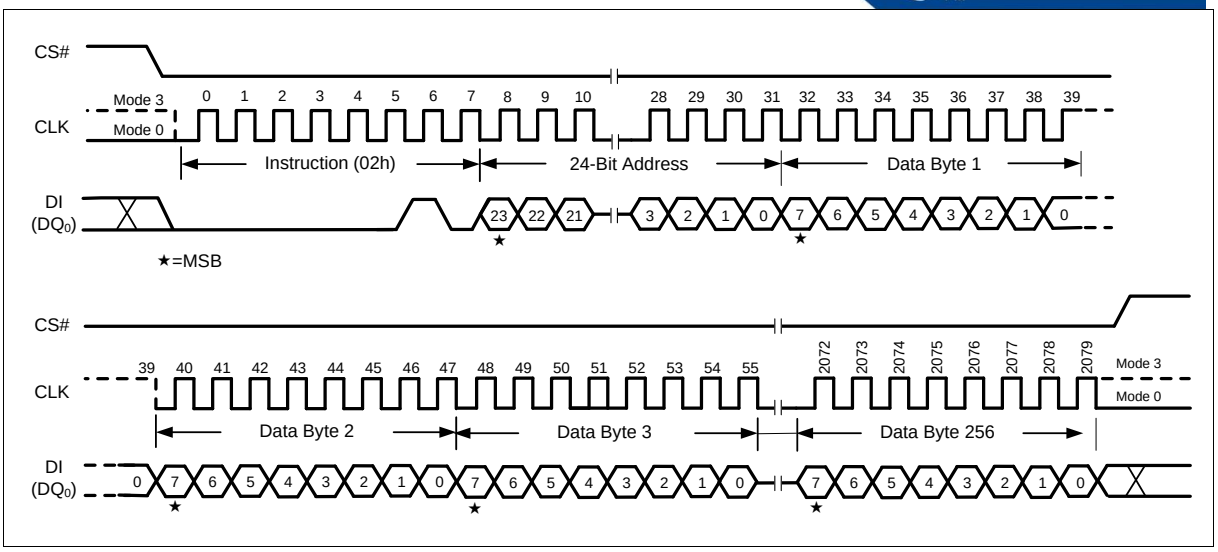


Figure 37 Page Program Command (SPI Mode)

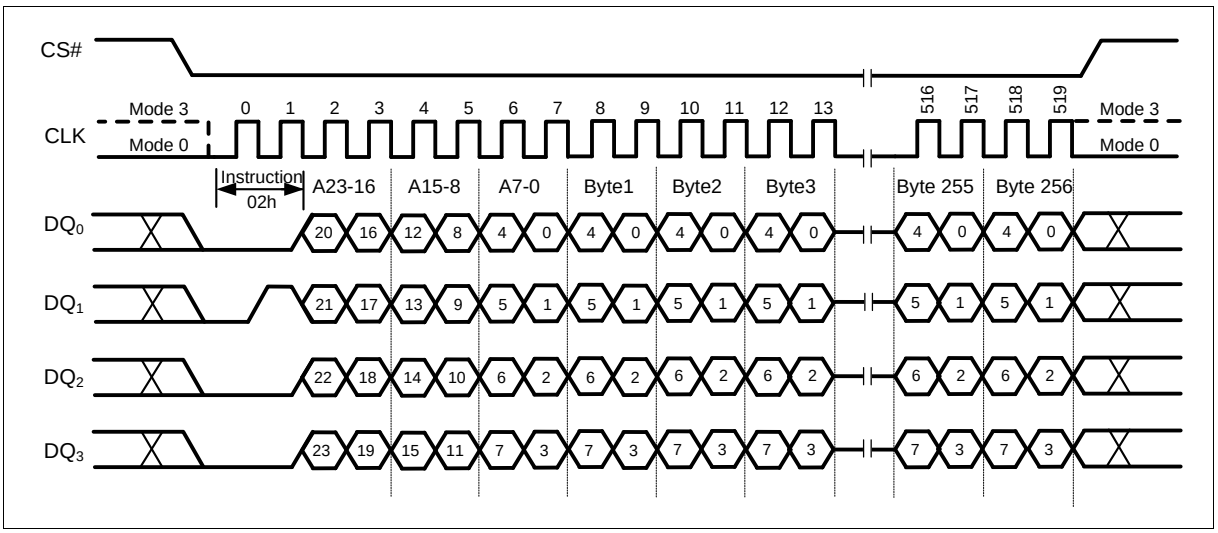


Figure 38 Page Program Command (QPI Mode)

8.4.21 Quad Input Page Program (32h)

The Quad Page Program command allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: DQ_0, DQ_1, DQ_2, and DQ_3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program command since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable in Status Register-2 must be set (QE=1). A Write Enable command must be executed before the device will accept the Quad Page Program command (Status Register-1, WEL=1). The command is initiated by driving the CS# pin low then shifting the command code “32h” followed by a 24-bit address A23-A0 and at least one data byte, into the DQ pins. The CS# pin must be held low for the entire length of the command while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program command sequence is shown in Figure 39.

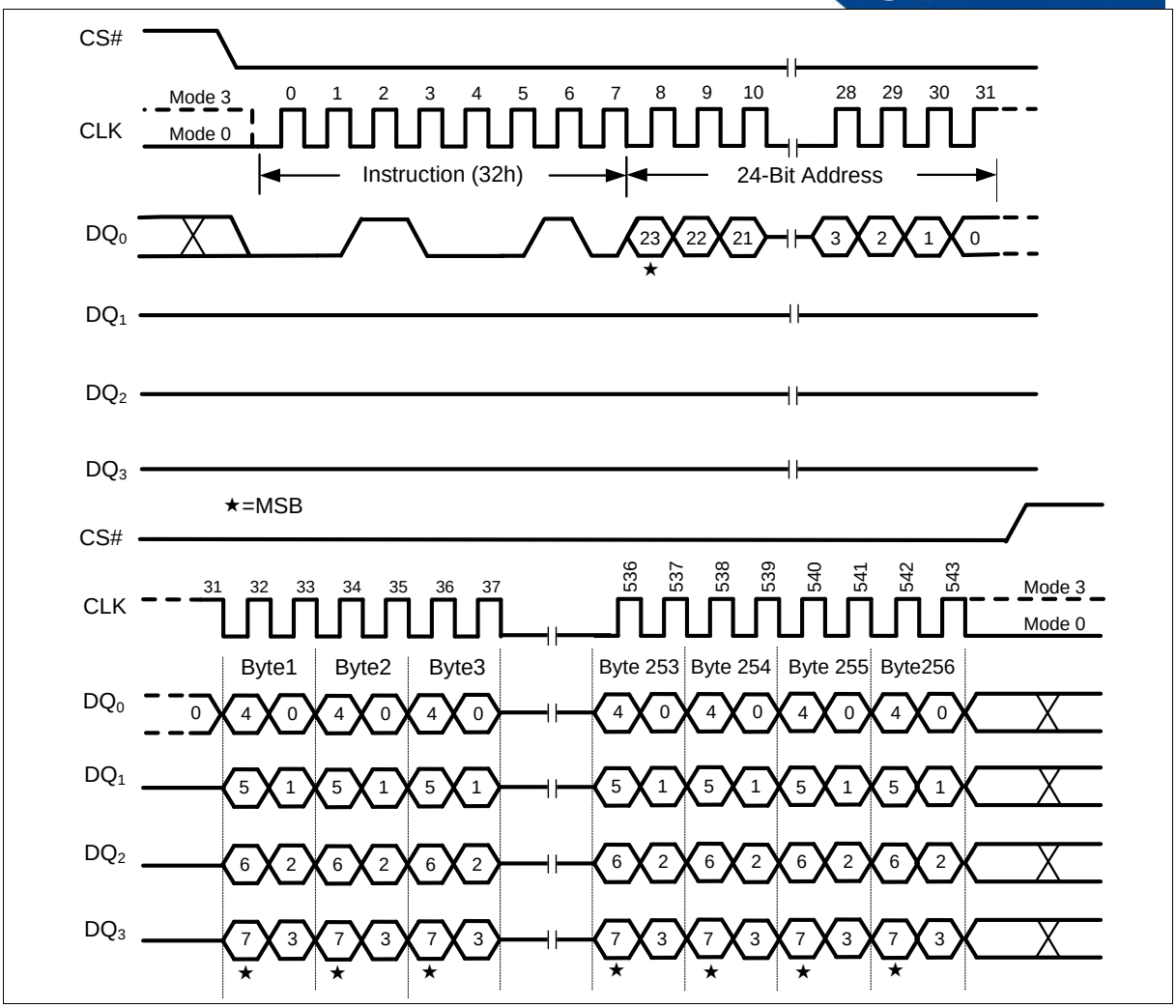


Figure 39 Quad Input Page Program Command (SPI Mode only)

8.4.22 Sector Erase (20h)

The Sector Erase command sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable command must be executed before the device will accept the Sector Erase Command (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the command code “20h” followed a 24-bit sector address A23-A0 (see Table 1). The Sector Erase command sequence is shown in Figure 40 & Figure 41.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase command will not be executed. After CS# is driven high, the self-timed Sector Erase command will commence for a time duration of t_{SE} (See “11.2.3 AC Characteristics”). While the Sector Erase cycle is in progress, the Read Status Register command may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase command will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (see Table 3 Status Register Memory Protection table).

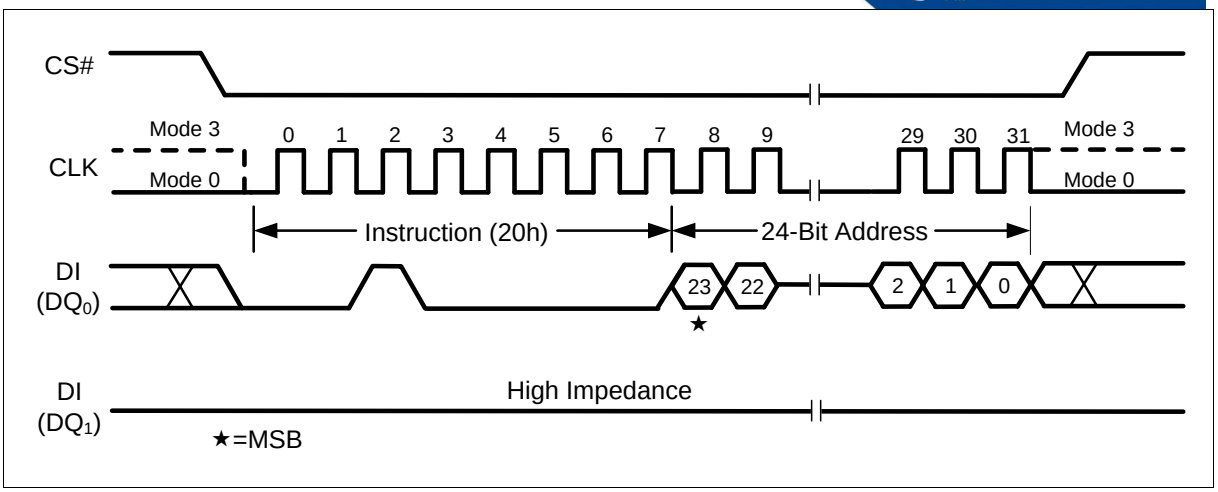


Figure 40 Sector Erase Command (SPI Mode)

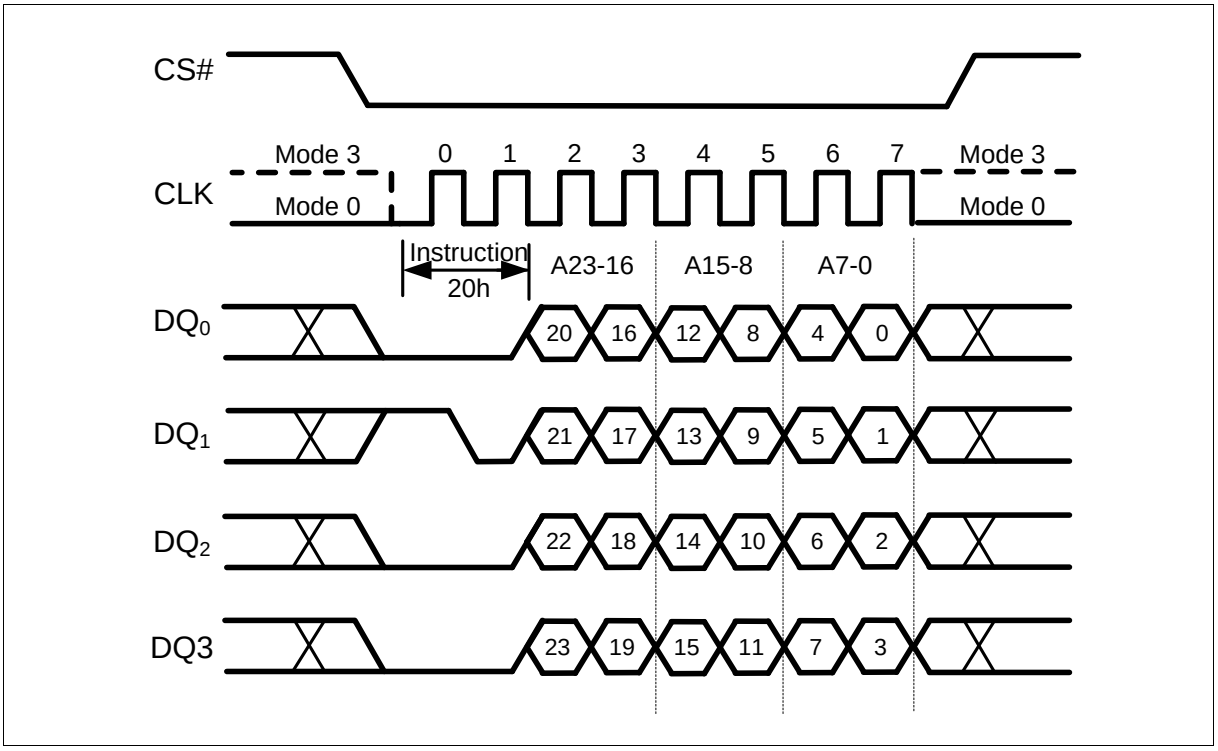


Figure 41 Sector Erase Command (QPI Mode)

8.4.23 32KB Block Erase (BE32) (52h)

The 32KB Block Erase command sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable command must be executed before the device will accept the Block Erase Command (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the command code “52h” followed a 24-bit block address A23-A0. The Block Erase command sequence is shown in Figure 42 & Figure 43.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase command will not be executed. After CS# is driven high, the self-timed Block Erase command will commence for a time duration of t_{BE1} (See “11.2.3 AC Characteristics”). While the Block Erase cycle is in progress, the Read Status Register command may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Block Erase cycle

and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase command will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (see Table 3 Status Register Memory Protection table).

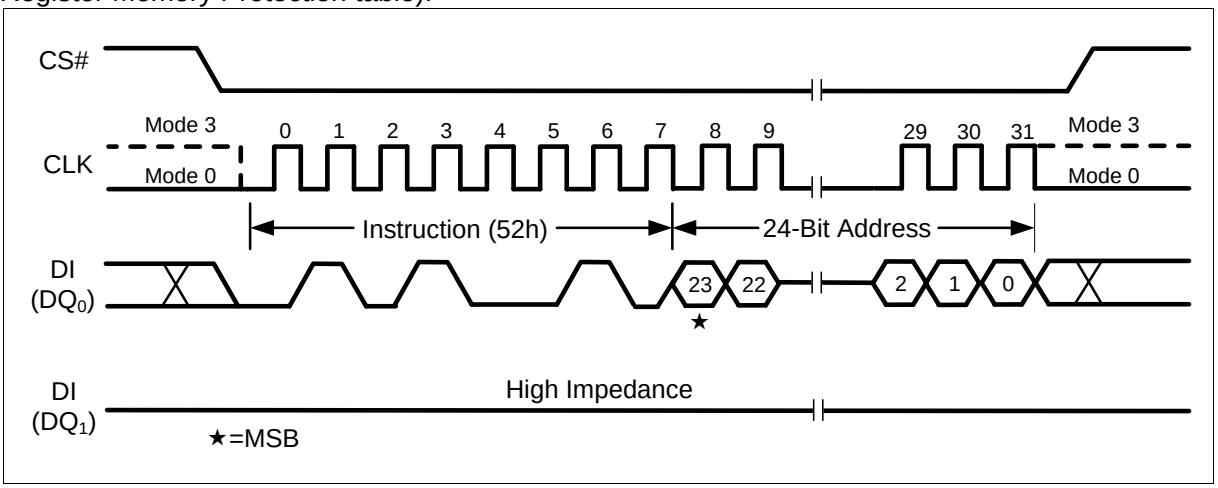


Figure 42 32KB Block Erase Command (SPI Mode)

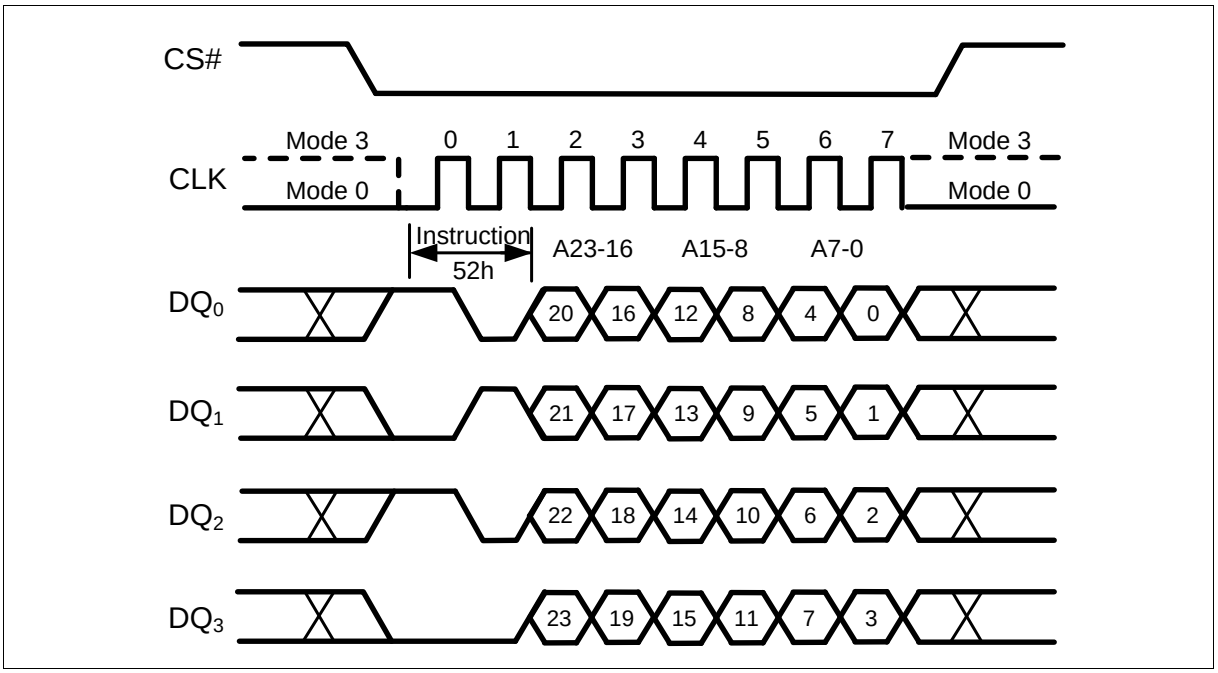


Figure 43 32KB Block Erase Command (QPI Mode)

8.4.24 64KB Block Erase (BE) (D8h)

The 64KB Block Erase command sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable command must be executed before the device will accept the Block Erase Command (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the command code “D8h” followed a 24-bit block address A23-A0. The Block Erase command sequence is shown in Figure 44 & Figure 45.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase command will not be executed. After CS# is driven high, the self-timed Block Erase command will commence for a time duration of t_{BE} (See “11.2.3 AC Characteristics”).

While the Block Erase cycle is in progress, the Read Status Register command may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase command will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits (see Table 3 Status Register Memory Protection table).

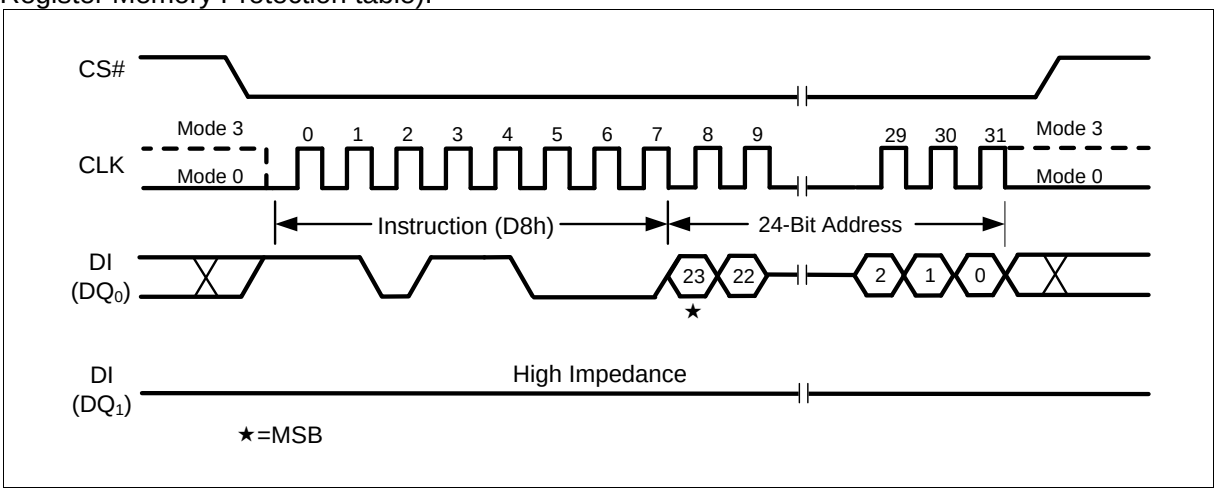


Figure 44 64KB Block Erase Command (SPI Mode)

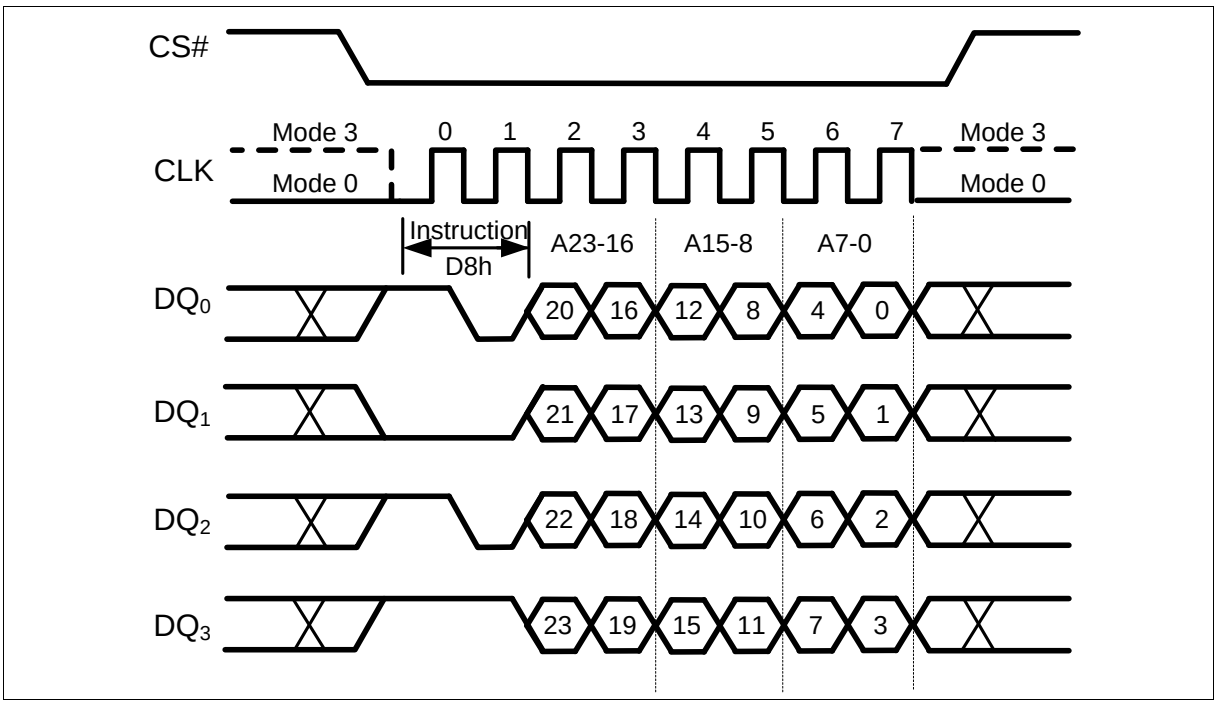


Figure 45 64KB Block Erase Command (QPI Mode)

8.4.25 Chip Erase (CE) (C7h / 60h)

The Chip Erase command sets all memory within the device to the erased state of all 1s (FFh). A Write Enable command must be executed before the device will accept the Chip Erase Command (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the command code “C7h” or “60h”. The Chip Erase command sequence is shown in Figure 46.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase command will not be executed. After CS# is driven high, the self-timed Chip Erase command will commence for a time duration of t_{CE} (See “11.2.3 AC Characteristics”). While the Chip Erase cycle is in progress, the Read Status Register command may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other commands again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase command will not be executed if any page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits.

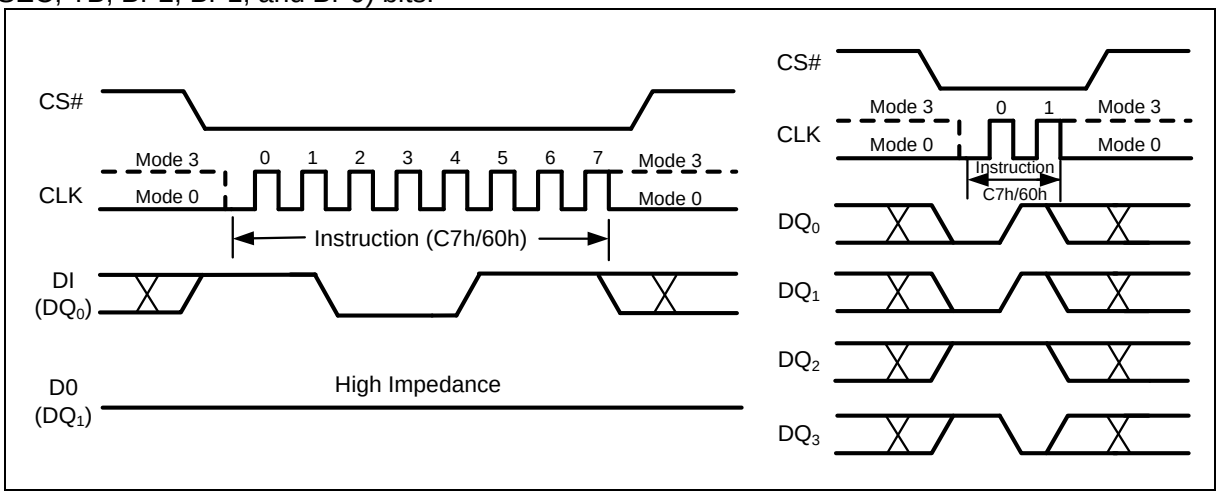


Figure 46 Chip Erase Command for SPI Mode (left) or QPI Mode (right)

8.4.26 Erase / Program Suspend (75h)

The Erase/Program Suspend command “75h”, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program/erase data to, any other sectors or blocks. The Erase/Program Suspend command sequence is shown in Figure 47 & Figure 48.

The Write Status Register command (01h) and Erase commands (20h, 52h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend command is ignored. The Write Status Register command (01h) and Program commands (02h, 32h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program or Quad Page Program operation.

The Erase/Program Suspend command “75h” will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the WIP bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the WIP bit equals to 0, the Suspend command will be ignored by the device. A maximum of time of “t_{SUS}” (See” 11.2.3 AC Characteristics”) is required to suspend the erase or program operation. The WIP bit in the Status Register will be cleared from 1 to 0 within “t_{SUS}” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend command “75h” is not issued earlier than a

minimum of time of "t_{SUS}" following the preceding Resume command "7Ah".

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.

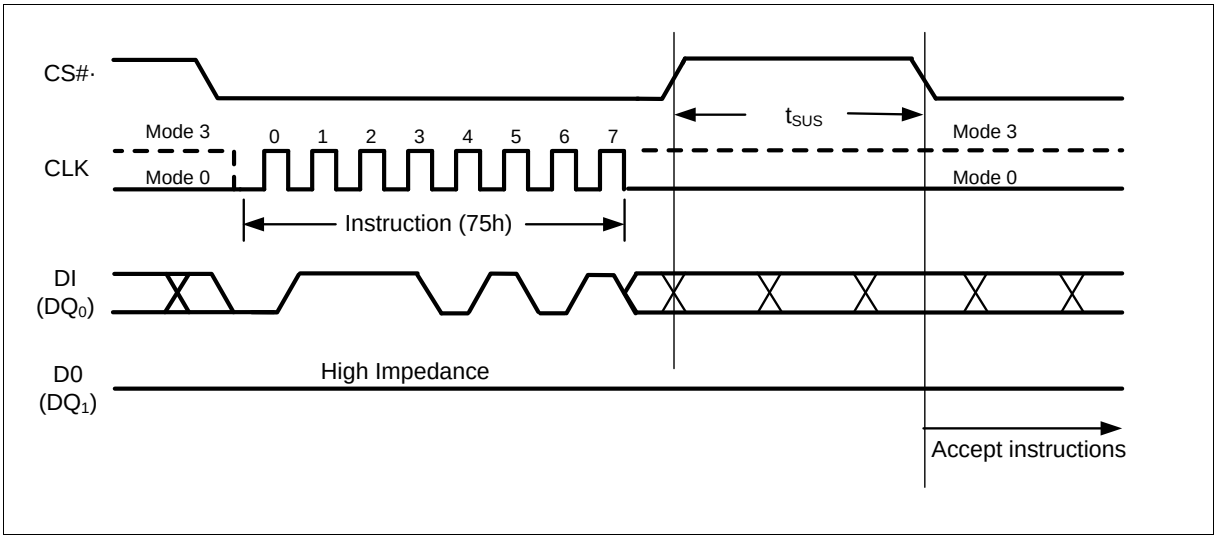


Figure 47 Erase/Program Suspend Command (SPI Mode)

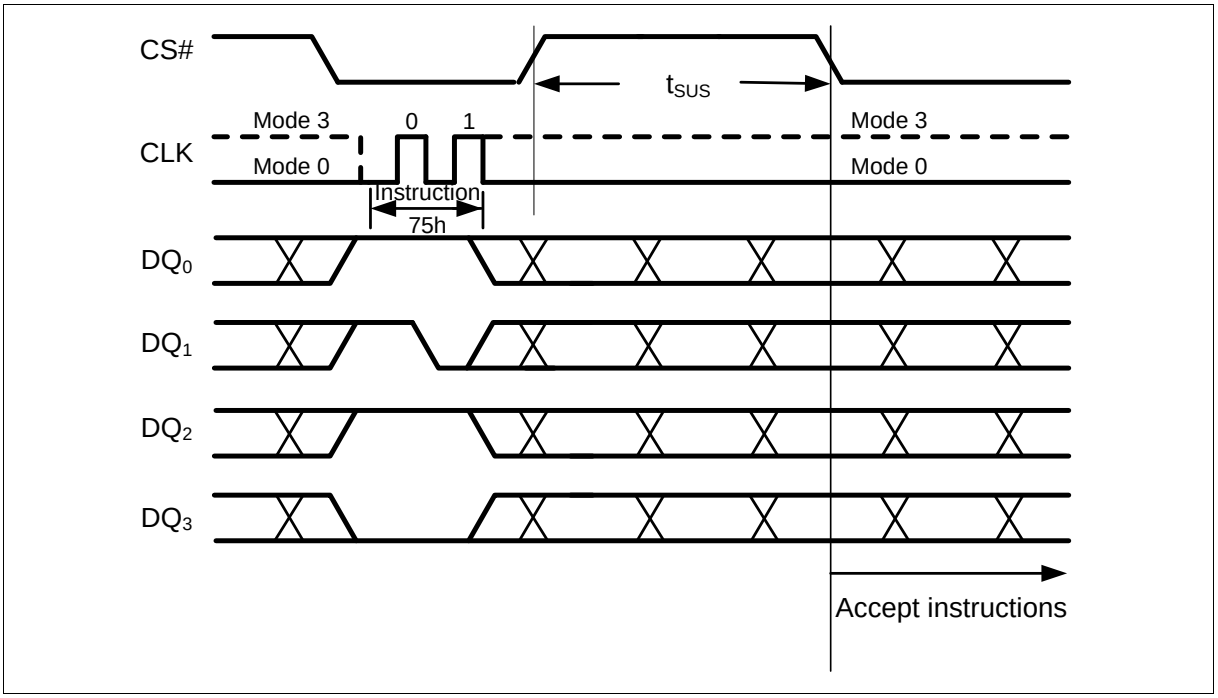


Figure 48 Erase/Program Suspend Command (QPI Mode)

8.4.27 Erase / Program Resume (7Ah)

The Erase/Program Resume command “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume command “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the WIP bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the WIP bit equals to 1, the Resume command “7Ah” will be ignored by the device. The Erase/Program Resume command sequence is shown in Figure 49 & Figure 50.

Resume command is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend command not to be issued within a minimum of time of “t_{SUS}” following a previous Resume command.

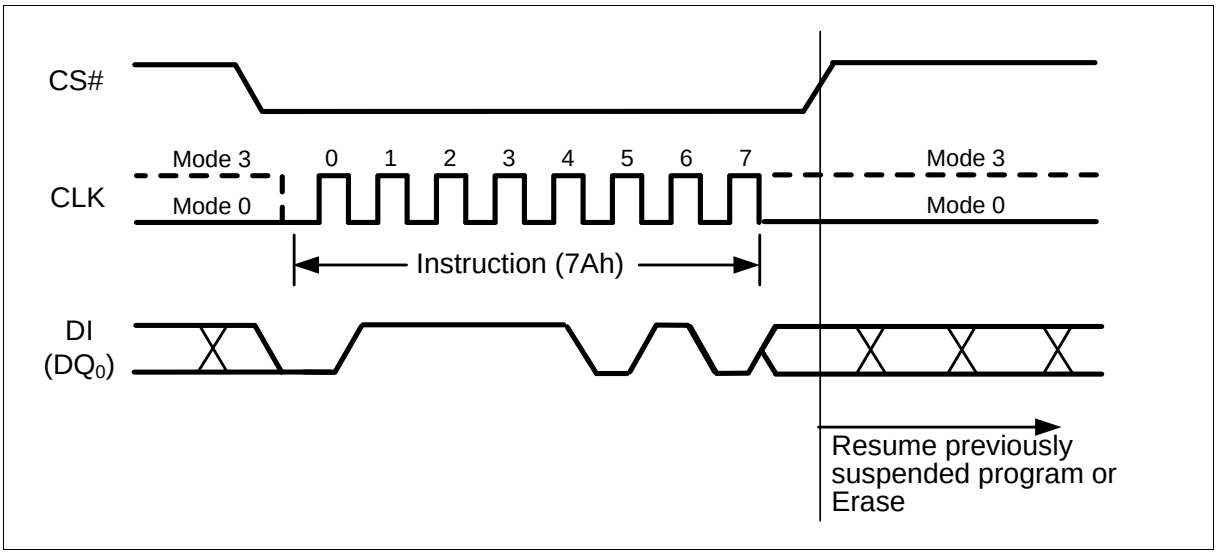


Figure 49 Erase/Program Resume Command (SPI Mode)

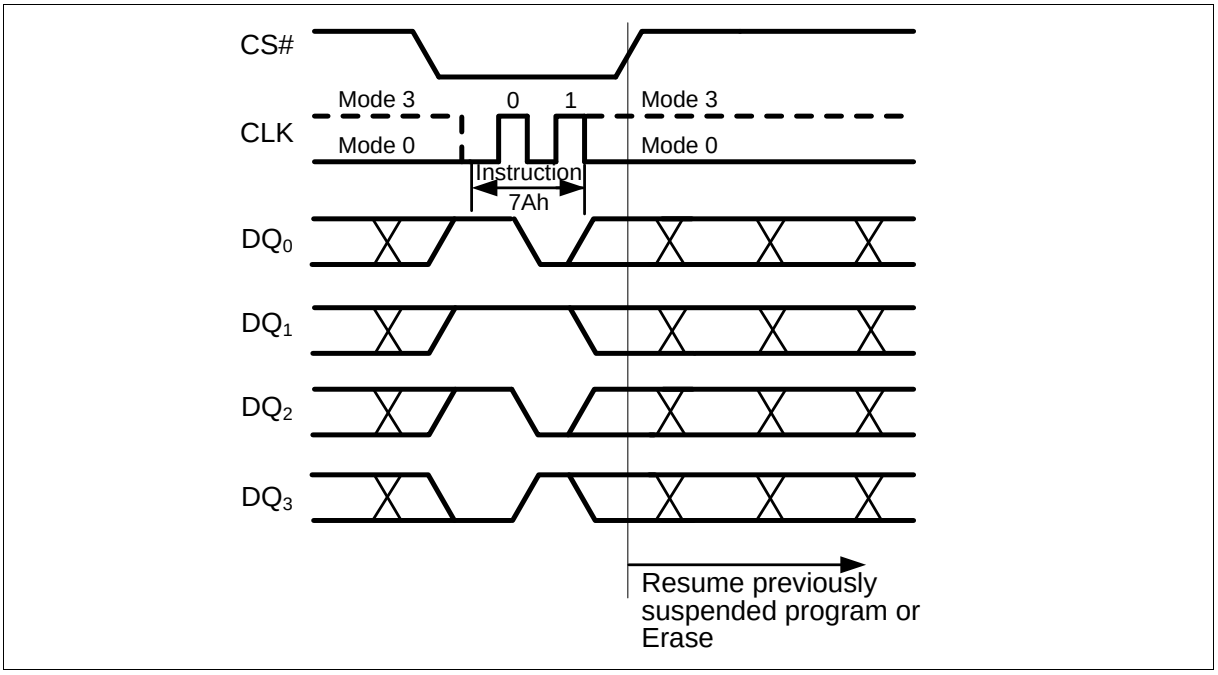


Figure 50 Erase/Program Resume Command (QPI Mode)

8.4.28 Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down command. The lower power consumption makes the Power-down command especially useful for battery powered applications (See I_{CC1} and I_{CC2} in "11.2.2 DC Characteristics"). The command is initiated by driving the CS# pin low and shifting the command code "B9h" as shown in Figure 51 & Figure 52.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Power-down command will not be executed. After CS# is driven high, the power-down state will enter within the time duration of t_{DP} (See "11.2.3_AC Characteristics"). While in the power-down state only the Release from Power- down / Device ID command, which restores the device to normal operation, will be recognized. All other commands are ignored. This includes the Read Status Register command, which is always available during normal operation. Ignoring all but one command makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of I_{CC1}.

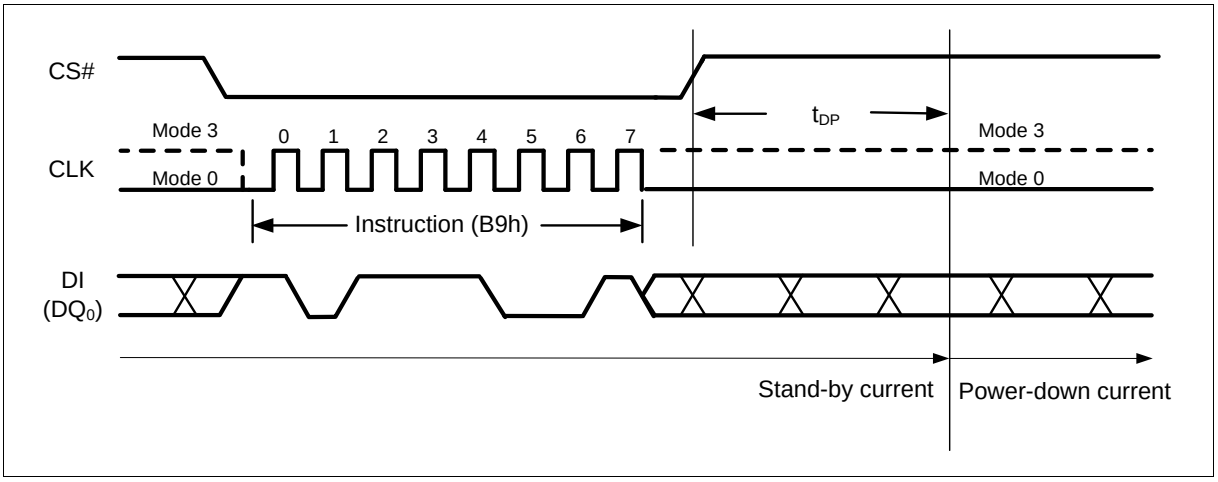


Figure 51 Deep Power-down Command (SPI Mode)

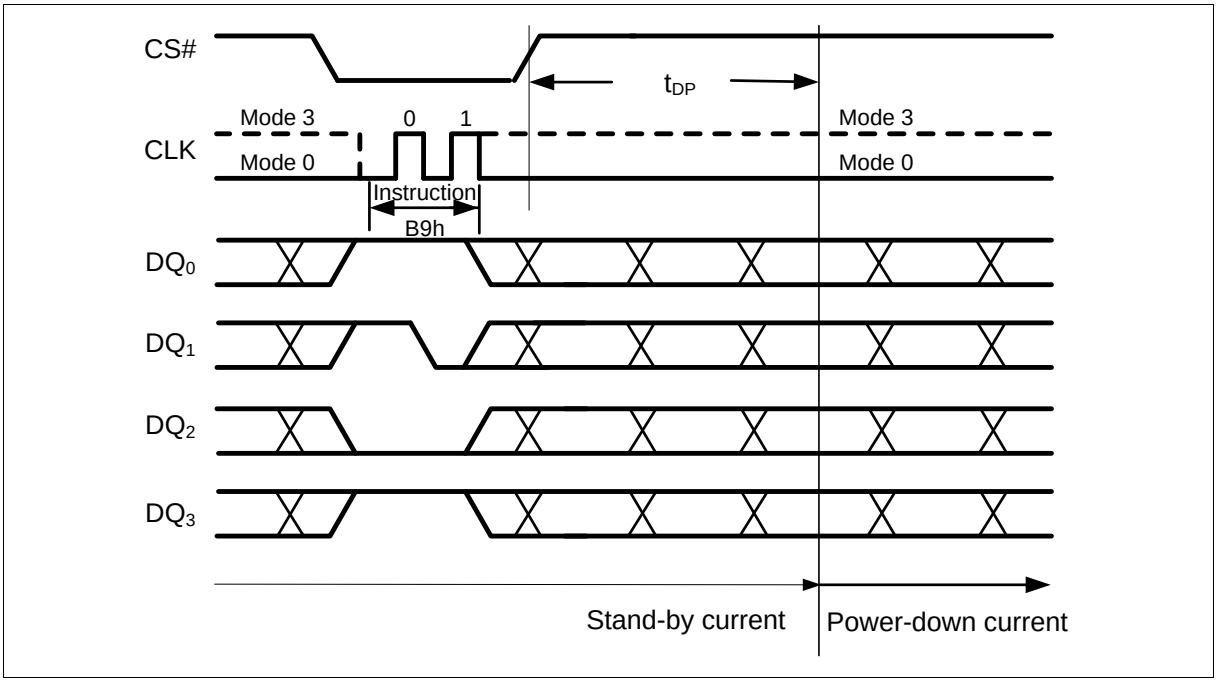


Figure 52 Deep Power-down Command (QPI Mode)

8.4.29 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID command is a multi-purpose command. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power-down state, the command is issued by driving the CS# pin low, shifting the command code “ABh” and driving CS# high as shown in Figure 53 & Figure 54. Release from power-down will take the time duration of t_{RES1} (See “11.2.3_AC Characteristics”) before the device will resume normal operation and other commands are accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the command is initiated by driving the CS# pin low and shifting the command code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 53 & Figure 54. The Device ID value for the FM25NQ04TX is listed in Table 23 Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the power-down state and obtain the Device ID, the command is the same as previously described, and shown in Figure 55 & Figure 56, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See “11.2.3_AC Characteristics”). After this time duration the device will resume normal operation and other commands will be accepted. If the Release from Power-down / Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equals 1) the command is ignored and will not have any effect on the current cycle.

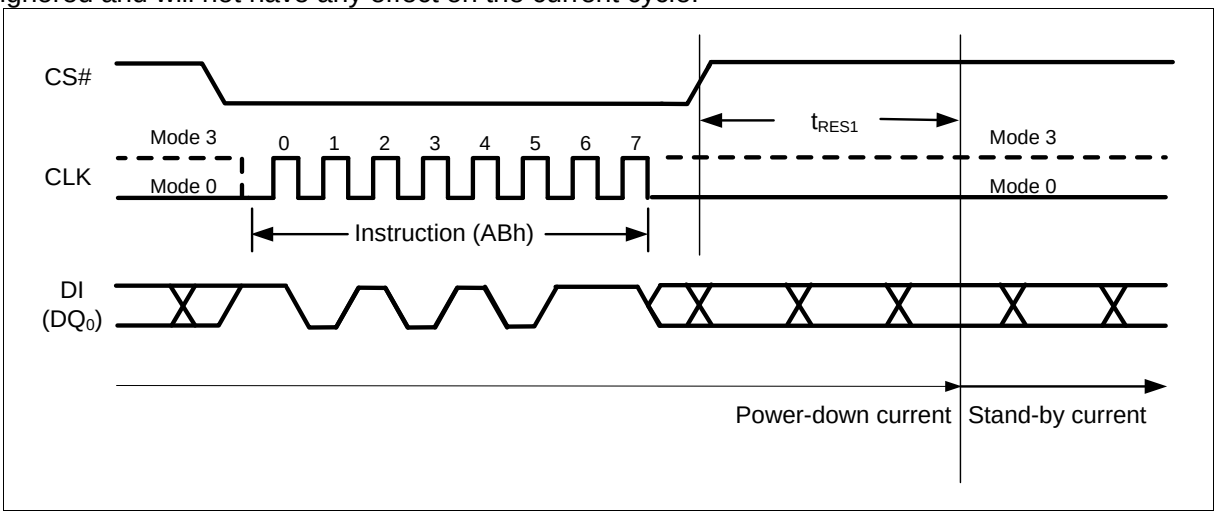


Figure 53 Release Power-down Command (SPI Mode)

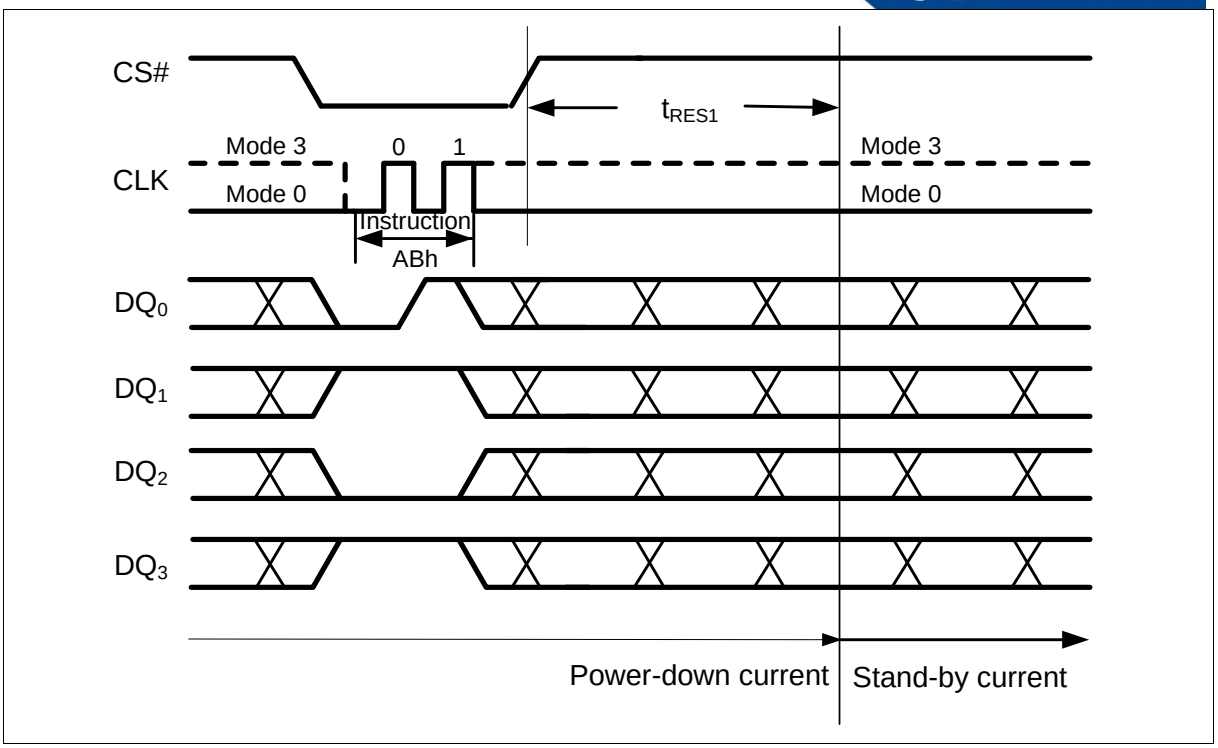


Figure 54 Release Power-down Command (QPI Mode)

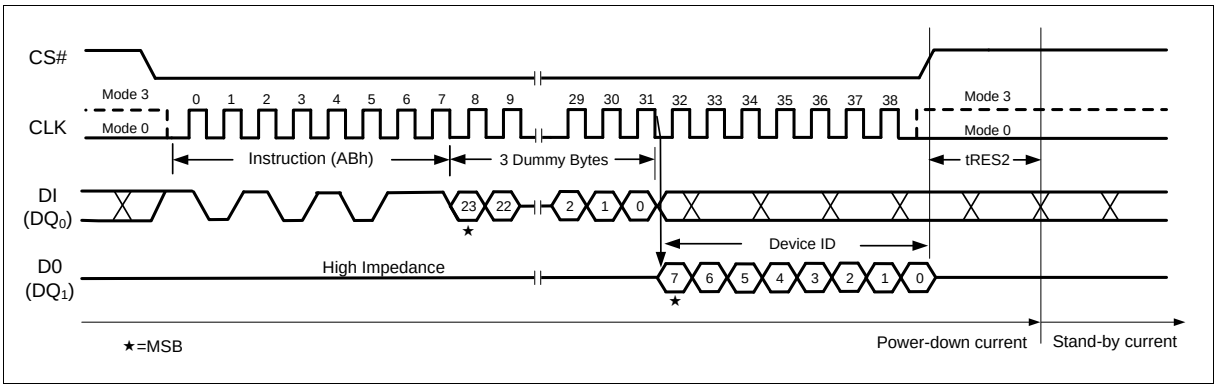


Figure 55 Release Power-down / Device ID Command (SPI Mode)

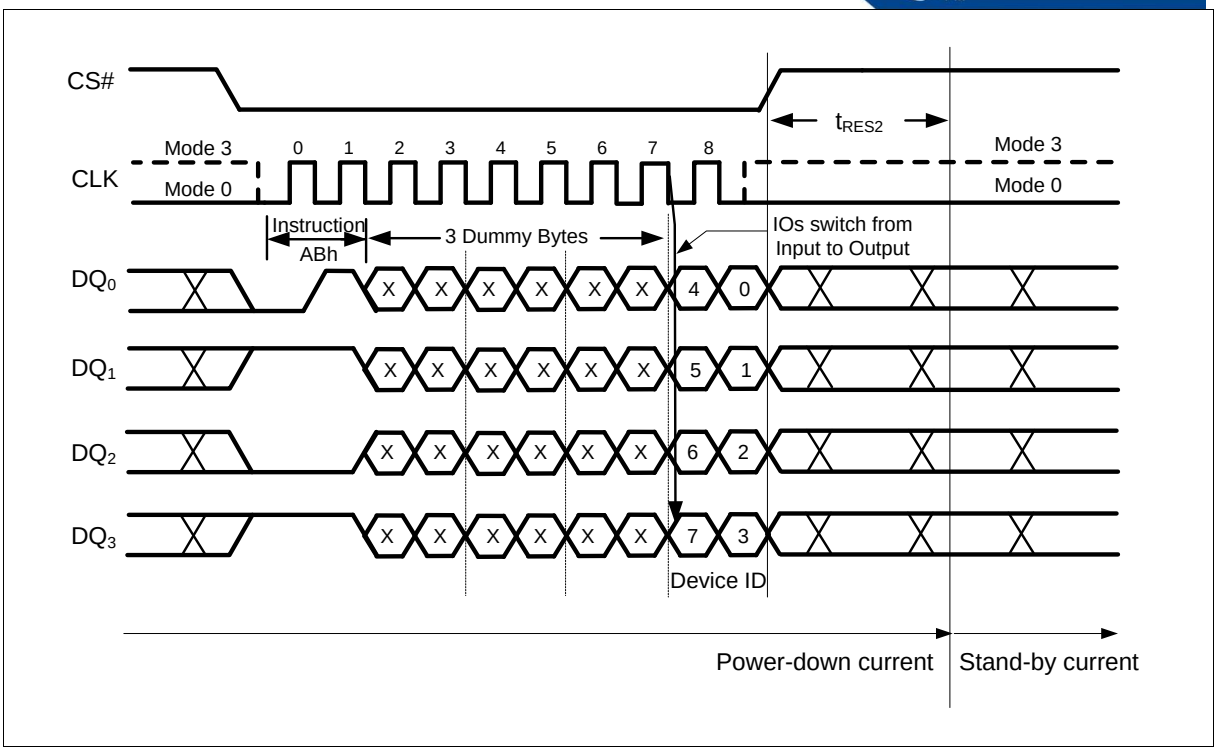


Figure 56 Release Power-down / Device ID Command (QPI Mode)

8.4.30 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-down / Device ID command that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID command is very similar to the Release from Power-down / Device ID command. The command is initiated by driving the CS# pin low and shifting the command code “90h” followed by a 24-bit address A23-A0 of 000000h. After which, the Manufacturer ID for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 57 & Figure 58. The Device ID value for the FM25NQ04TX is listed in Table 23 Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The command is completed by driving CS# high.

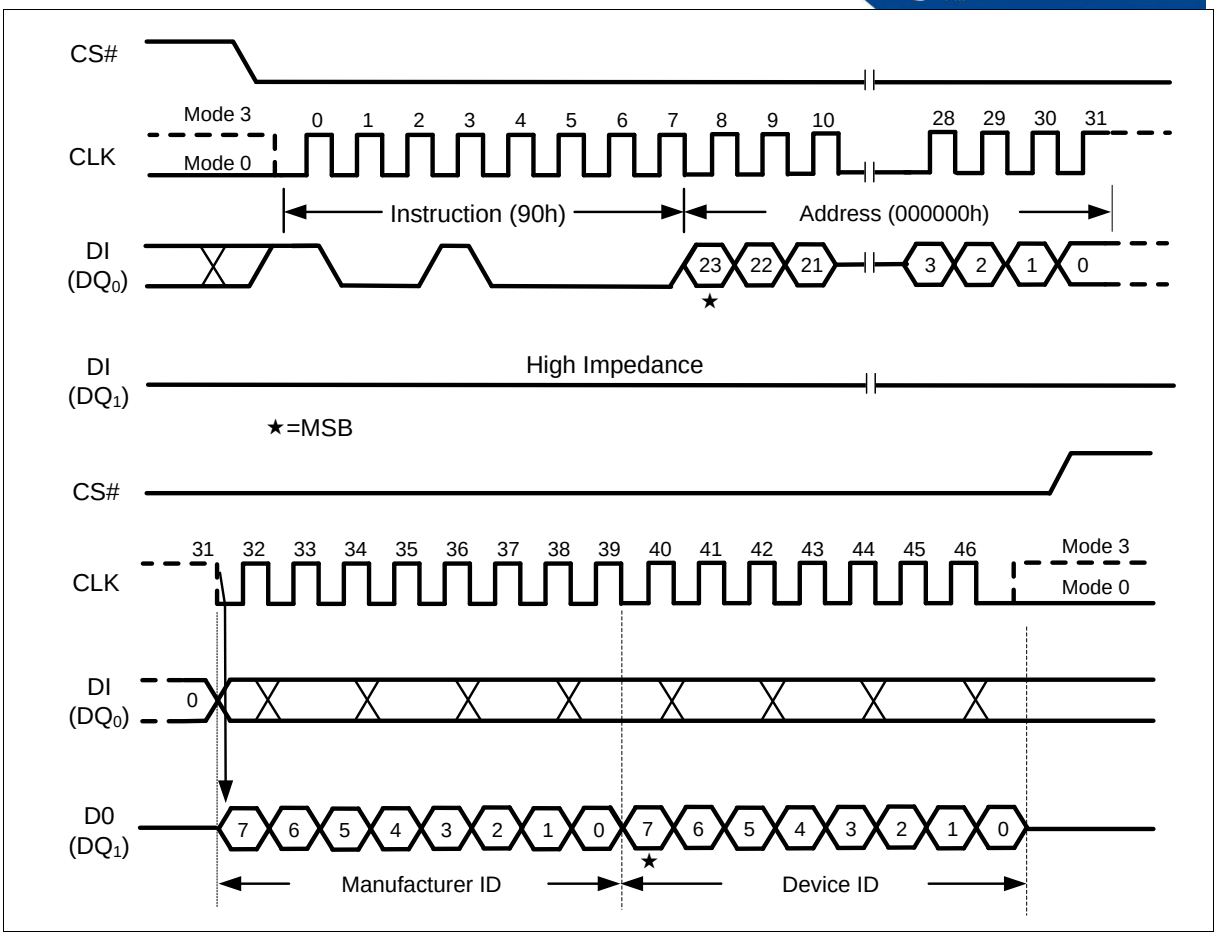


Figure 57 Read Manufacturer / Device ID Command (SPI Mode)

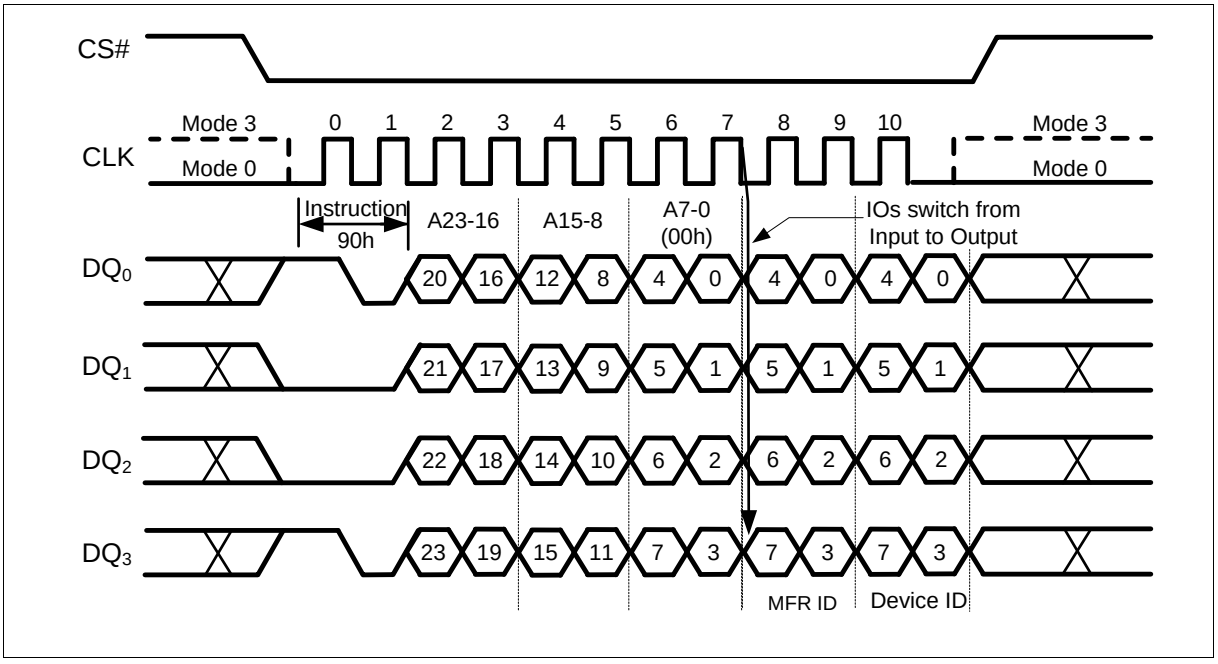


Figure 58 Read Manufacturer / Device ID Command (QPI Mode)

8.4.31 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O command is an alternative to the Read Manufacturer / Device ID command that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O command is similar to the Fast Read Dual I/O command. The command is initiated by driving the CS# pin low and shifting the command code "92h" followed by a 24-bit address A23-A0 of 000000h, 8-bit Continuous Read Mode Bits, with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in Figure 59. The Device ID value for the FM25NQ04TX is listed in Table 23 Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The command is completed by driving CS# high.

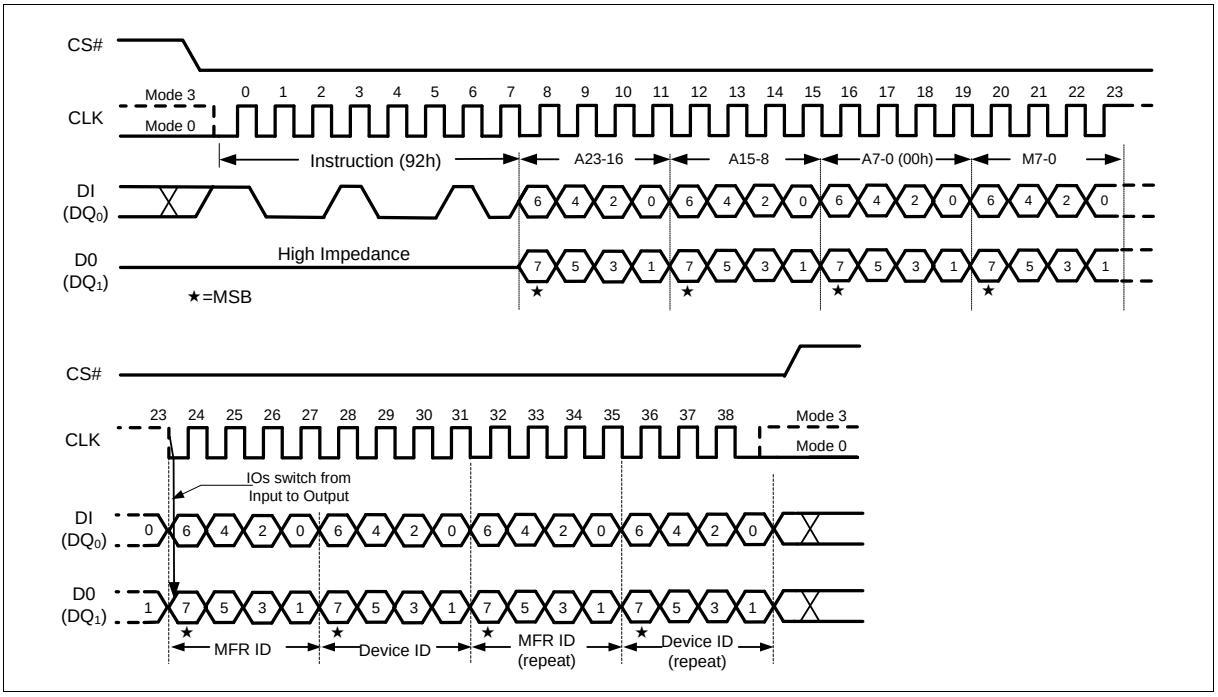


Figure 59 Read Manufacturer / Device ID Dual I/O Command (SPI Mode only)

Note:
The "Continuous Read Mode" bits M7-M0 must be set to Fxh to be compatible with Fast Read Dual I/O command.

8.4.32 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O command is an alternative to the Read Manufacturer / Device ID command that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O command is similar to the Fast Read Quad I/O command. The command is initiated by driving the CS# pin low and shifting the command code "94h" followed by a 24-bit address A23-A0 of 000000h, 8-bit Continuous Read Mode Bits and then four clock dummy cycles, with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 60. The Device ID value for the FM25NQ04TX is listed in

Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The command is completed by driving CS# high.

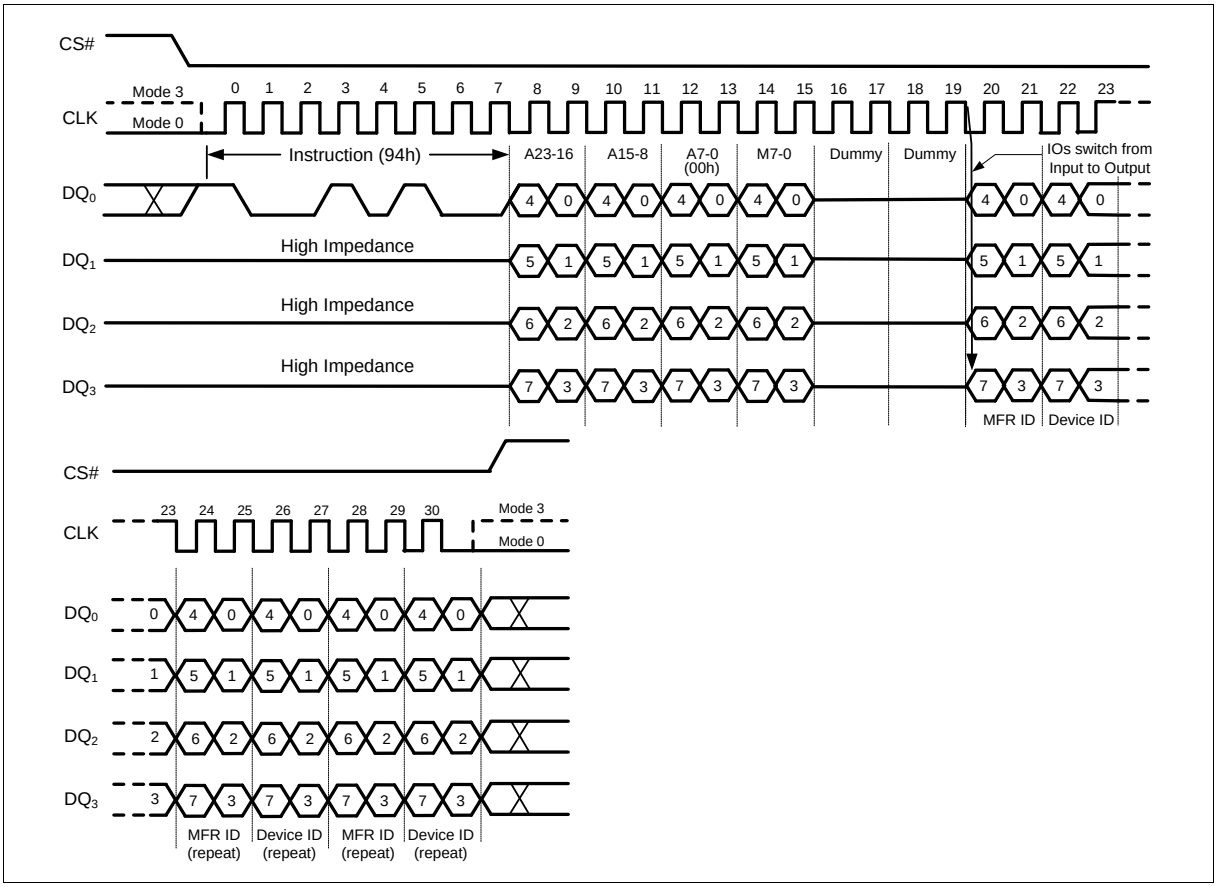


Figure 60 Read Manufacturer / Device ID Quad I/O Command (SPI Mode only)

Note:
The “Continuous Read Mode” bits M7-M0 must be set to Fxh to be compatible with Fast Read Quad I/O command.

8.4.33 Read Unique ID Number (4Bh)

The Read Unique ID Number command accesses a factory-set read-only 64-bit number that is unique to each FM25NQ04TX device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID command is initiated by driving the CS# pin low and shifting the command code “4Bh” followed by a four bytes of dummy clocks. After which, the 64- bit ID is shifted out on the falling edge of CLK as shown in Figure 61.

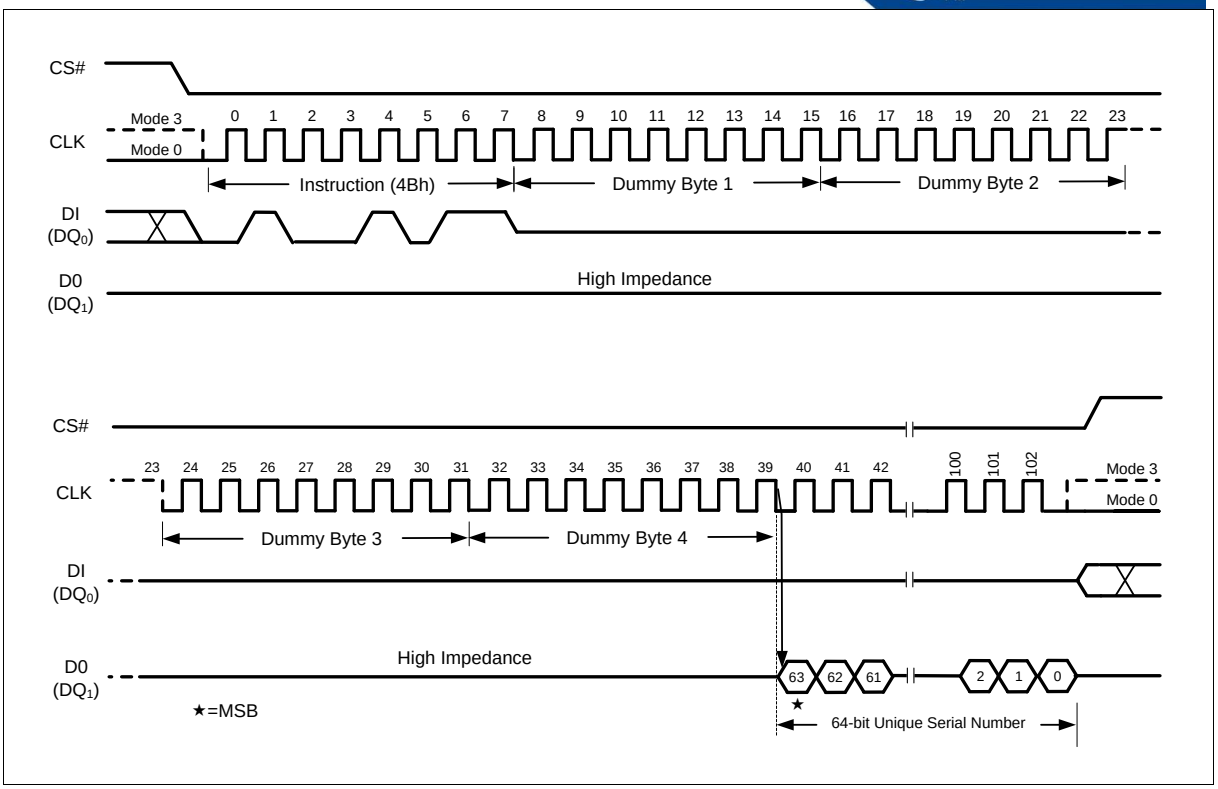


Figure 61 Read Unique ID Number Command (SPI Mode only)

8.4.34 Read JEDEC ID (9Fh)

For compatibility reasons, the FM25NQ04TX provides several commands to electronically determine the identity of the device. The Read JEDEC ID command is compatible with the JEDEC standard for SPI compatible serial memories. The command is initiated by driving the CS# pin low and shifting the command code “9Fh”. The JEDEC assigned Manufacturer ID byte for Shanghai Fudan Microelectronics Group Co., Ltd (A1h) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity ID7-ID0 are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 62 & Figure 63. For memory type and capacity values refer to Table 23 Manufacturer and Device Identification table.

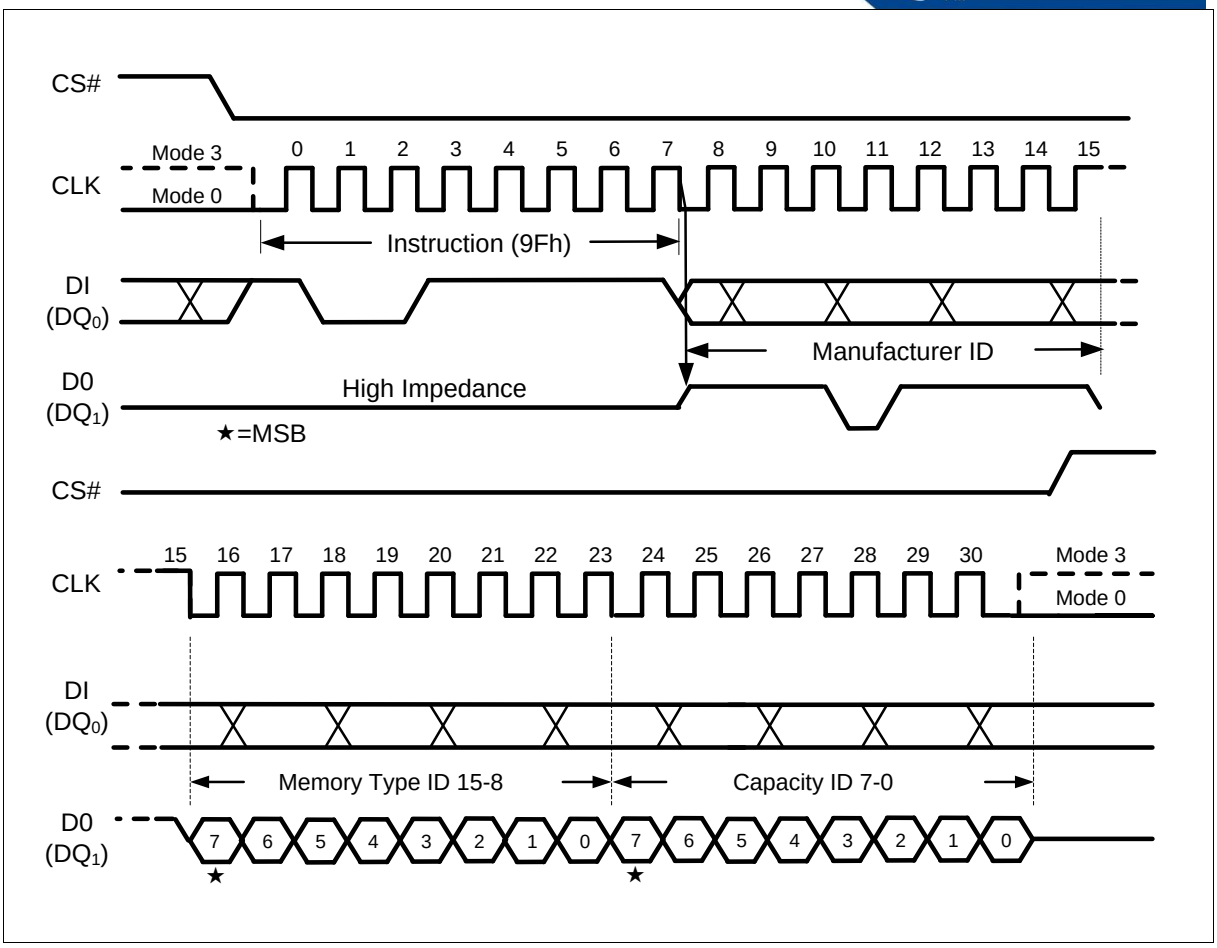


Figure 62 Read JEDEC ID Command (SPI Mode)

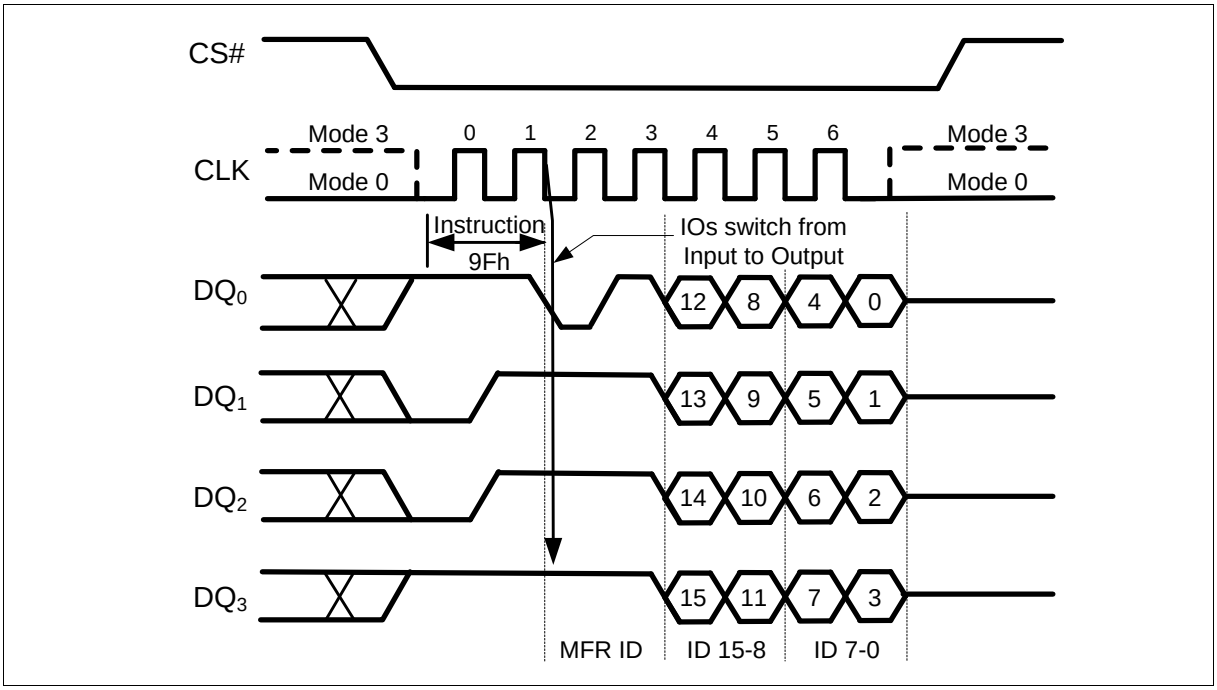


Figure 63 Read JEDEC ID Command (QPI Mode)

8.4.35 Read SFDP Register (5Ah)

The FM25NQ04TX features a 256-Byte Serial Flash Discoverable Parameter (SFDP) register that contains information about device configurations, available commands and other features. The SFDP parameters are stored in one or more Parameter Identification (PID) tables. Currently only one PID table is specified, but more may be added in the future. The Read SFDP Register command is compatible with the SFDP standard initially established in 2010 for PC and other applications, as well as the JEDEC standard 1.0 that is published in 2011.

The Read SFDP command is initiated by driving the /CS pin low and shifting the command code "5Ah" followed by a 24-bit address (A23-A0)(1) into the DI pin. Eight "dummy" clocks are also required before the SFDP register contents are shifted out on the falling edge of the 40th CLK with most significant bit (MSB) first as shown in Figure 64. For SFDP register values and descriptions, refer to the following SFDP Definition table.

Note: 1. A23-A8 = 0; A7-A0 are used to define the starting byte address for the 256-Byte SFDP Register.

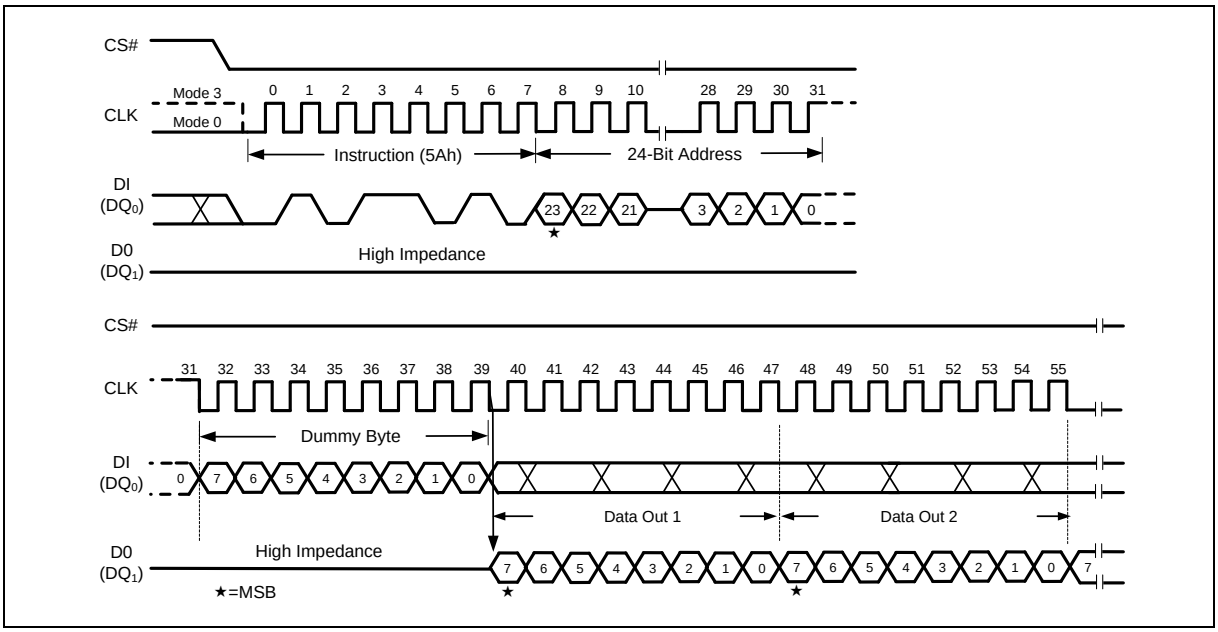


Figure 64 Read SFDP Register Command

Serial Flash Discoverable Parameter (JEDEC Revision 1.0) Definition Table

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
00h	53h	SFDP Signature	SFDP Signature = 50444653h
01h	46h	SFDP Signature	
02h	44h	SFDP Signature	
03h	50h	SFDP Signature	
04h	00h	SFDP Minor Revision Number	JEDEC Revision 1.0
05h	01h	SFDP Major Revision Number	
06h	00h	Number of Parameter Headers (NPH)	1 Parameter Header
07h	FFh	Reserved	
08h	00h	PID(3)(0): ID Number	00h = JEDEC specified
09h	00h	PID(0): Parameter Table Minor Revision Number	JEDEC Revision 1.0
0Ah	01h	PID(0): Parameter Table Major Revision Number	

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
0Bh	09h	PID(0): Parameter Table Length	9 Dwords[2]
0Ch	80h	PID(0): Parameter Table Pointer (PTP) (A7-A0)	PID(0) Pointer = 000080h
0Dh	00h	PID(0): Parameter Table Pointer (PTP) (A15-A8)	
0Eh	00h	PID(0): Parameter Table Pointer (PTP) (A23-A16)	
0Fh	FFh	Reserved	
10h	FFh	Reserved	
...[1]	FFh	Reserved	
7Fh	FFh	Reserved	
80h	E5h	Bit[7:5]=111 Reserved Bit[4:3]=00 Non-volatile Status Register Bit[2]=1 Page Programmable Bit[1:0]=01 Supports 4KB Erase	
81h	20h	4K-Byte Erase Opcode	
82h	F1h	Bit[7] =1 Reserved Bit[6] =1 Supports (1-1-4) Fast Read Bit[5] =1 Supports (1-4-4) Fast Read Bit[4] =1 Supports (1-2-2) Fast Read Bit[3] =0 Not support Dual Transfer Rate Bit[2:1]=00 3-Byte/24-Bit Only Addressing Bit[0] =1 Supports (1-1-2) Fast Read	
83h	FFh	Reserved	
84h	FFh	Flash Size in Bits	32 Mega Bits = 01FFFFFFh
85h	FFh	Flash Size in Bits	
86h	FFh	Flash Size in Bits	
87h	01h	Flash Size in Bits	
88h	44h	Bit[7:5]=010 8 Mode Bits are needed Bit[4:0]=00100 16 Dummy Bits are needed	Fast Read Quad I/O Setting
89h	EBh	Quad Input Quad Output Fast Read Opcode	
8Ah	08h	Bit[7:5]=000 No Mode Bits are needed Bit[4:0]=01000 8 Dummy Bits are needed	Fast Read Quad Output Setting
8Bh	6Bh	Single Input Quad Output Fast Read Opcode	
8Ch	08h	Bit[7:5]=000 No Mode Bits are needed Bit[4:0]=01000 8 Dummy Bits are needed	Fast Read Dual Output Setting
8Dh	3Bh	Single Input Dual Output Fast Read Opcode	
8Eh	80h	Bit[7:5]=100 8 Mode bits are needed Bit[4:0]=00000 No Dummy bits are needed	Fast Read Dual I/O Setting
8Fh	BBh	Dual Input Dual Output Fast Read Opcode	
90h	FEh	Bit[7:5]=111 Reserved Bit[4]=1 support (4-4-4) Fast Read Bit[3:1]=111 Reserved Bit[0]=0 Not support (2-2-2) Fast Read	
91h	FFh	Reserved	
92h	FFh	Reserved	
93h	FFh	Reserved	
94h	FFh	Reserved	
95h	FFh	Reserved	
96h	00h	No Mode Bits or Dummy Bits for (2-2-2) Fast Read	
97h	00h	Not support (2-2-2) Fast Read	
98h	FFh	Reserved	
99h	FFh	Reserved	
9Ah	08h	Bit[7:5]=000 No Mode bits are needed Bit[4:0]=01000 8 Dummy bits are needed	

BYTE ADDRESS	DATA	DESCRIPTION	COMMENT
9Bh	EBh	QPI Fast Read Opcode	
9Ch	0Ch	Sector Type 1 Size (4KB)	Sector Erase Type & Opcode
9Dh	20h	Sector Type 1 Opcode	
9Eh	0Fh	Sector Type 2 Size (32KB)	
9Fh	52h	Sector Type 2 Opcode	
A0h	10h	Sector Type 3 Size (64KB)	Sector Erase Type & Opcode
A1h	D8h	Sector Type 3 Opcode	
A2h	00h	Sector Type 4 Size (256KB) – Not supported	
A3h	00h	Sector Type 4 Opcode – Not supported	
...(1)	FFh	Reserved	
FFh	FFh	Reserved	

Notes:
1. Data stored in Byte Address 10h to 7Fh & A4h to FFh are Reserved, the value is FFh.
2. 1 Dword = 4 Bytes
3. PID(x) = Parameter Identification Table (x)

8.4.36 Erase Security Sectors (44h)

The FM25NQ04TX offers two 512-byte Security Sectors which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Sector command is similar to the Sector Erase command. A Write Enable command must be executed before the device will accept the Erase Security Sector Command (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the command code “44h” followed by a 24-bit address A23-A0 to erase one of the two Security Sectors.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Sector #0	00h	0 0 0 0	0 0 0 0 0 0 0 1	Don’t Care
Security Sector #1	00h	0 0 0 1	0 0 0 0 0 0 0 1	Don’t Care

The Erase Security Sector command sequence is shown in Figure 65. The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the command will not be executed. After CS# is driven high, the self-timed Erase Security Sector operation will commence for a time duration of t_{SE} (See “11.2.3_AC Characteristics”). While the Erase Security Sector cycle is in progress, the Read Status Register command may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Erase Security Sector cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Sector Lock Bits (LB1-0) in the Status Register-2 can be used to OTP protect the Security Sectors. Once a lock bit is set to 1, the corresponding Security Sector will be permanently locked, Erase Security Sector command to that register will be ignored (See “0_The Error bit is a status flag, which shows the status of last Program/Erase operation. It will be set to "1", if the Program/Erase operation fails or the Program/Erase region is protected.

Security Sector Lock Bits (LB1,LB0)” for detail descriptions).

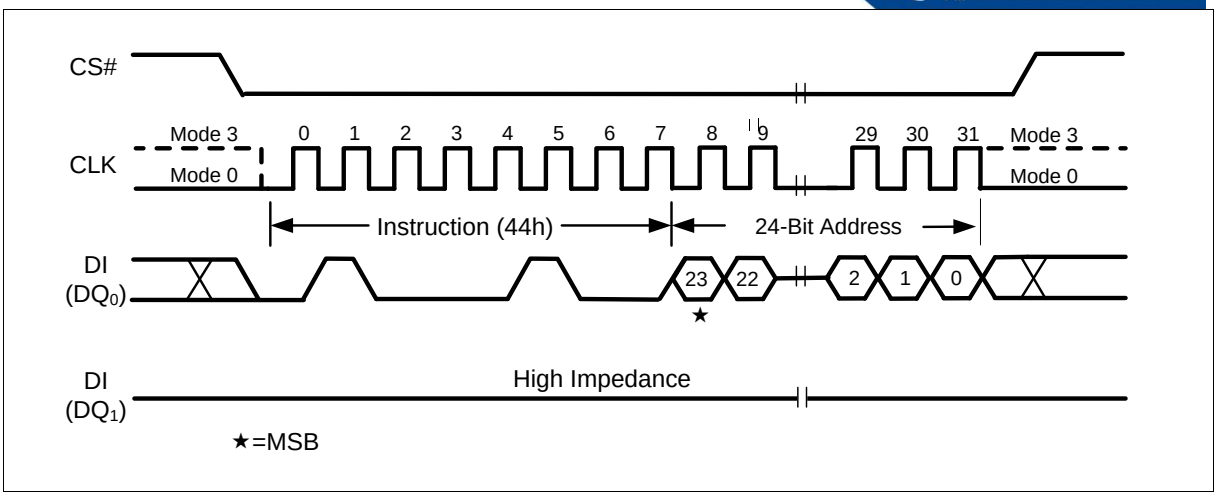


Figure 65 Erase Security Sectors Command (SPI Mode only)

8.4.37 Program Security Sectors (42h)

The Program Security Sector command is similar to the Page Program command. It allows from one byte to 256 bytes of Security Sector data to be programmed at previously erased (FFh) memory locations. A Write Enable command must be executed before the device will accept the Program Security Sector Command (Status Register bit WEL= 1). The command is initiated by driving the CS# pin low then shifting the command code “42h” followed by a 24-bit address A23-A0 and at least one data byte, into the DI pin. The CS# pin must be held low for the entire length of the command while data is being sent to the device.

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Sector #0	00h	0 0 0 0	0 0 0 0 0 0 0 1	Byte Address
Security Sector #1	00h	0 0 0 1	0 0 0 0 0 0 0 1	Byte Address

The Program Security Sector command sequence is shown in Figure 66. The Security Sector Lock Bits (LB1-0) in the Status Register-2 can be used to OTP protect the Security Sectors. Once a lock bit is set to 1, the corresponding Security Sector will be permanently locked, Program Security Sector command to that register will be ignored (See “0_The Error bit is a status flag, which shows the status of last Program/Erase operation. It will be set to "1", if the Program/Erase operation fails or the Program/Erase region is protected.

Security Sector Lock Bits (LB1,LB0)”, “8.4.20_Page Program (02h)” for detail descriptions).

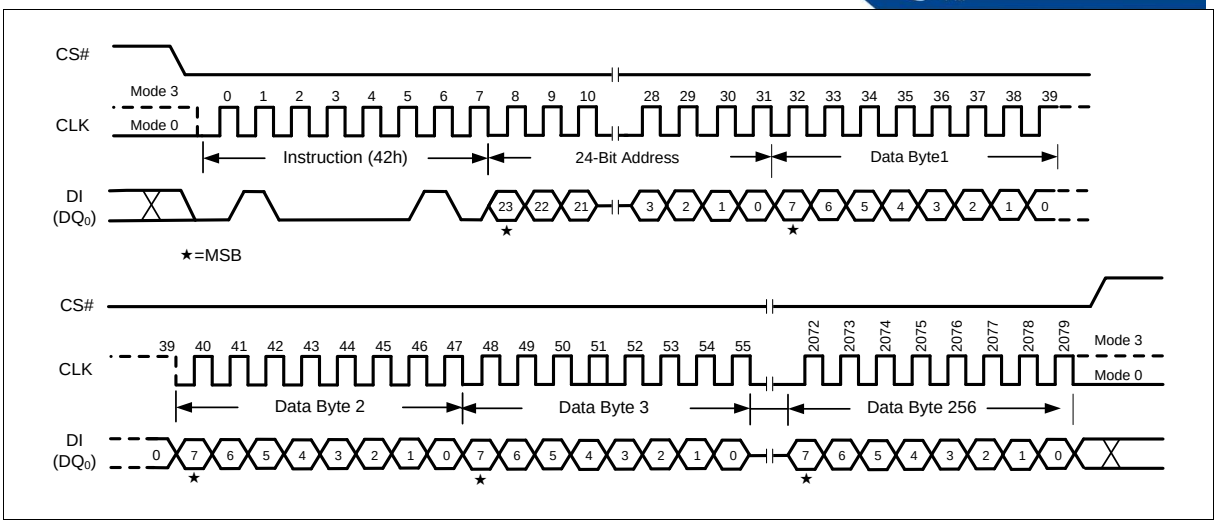


Figure 66 Program Security Sectors Command (SPI Mode only)

8.4.38 Read Security Sectors (48h)

The Read Security Sector command is similar to the Fast Read command and allows one or more data bytes to be sequentially read from one of the two Security Sectors. The command is initiated by driving the CS# pin low and then shifting the command code “48h” followed by a 24-bit address A23-A0 and eight “dummy” clocks into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte 1FFh), it will be reset to 00h, the first byte of the register, and continue to increment. The command is completed by driving CS# high. The Read Security Sector command sequence is shown in Figure 67. If a Read Security Sector command is issued while an Erase, Program or Write cycle is in process (WIP =1) the command is ignored and will not have any effect on the current cycle. The Read Security Sector command allows clock rates from D.C. to a maximum of FR (see “11.2.3 AC Characteristics”).

ADDRESS	A23-16	A15-12	A11-8	A7-0
Security Sector #0	00h	0 0 0 0	0 0 0 0 0 0 0 1	Byte Address
Security Sector #1	00h	0 0 0 1	0 0 0 0 0 0 0 1	Byte Address

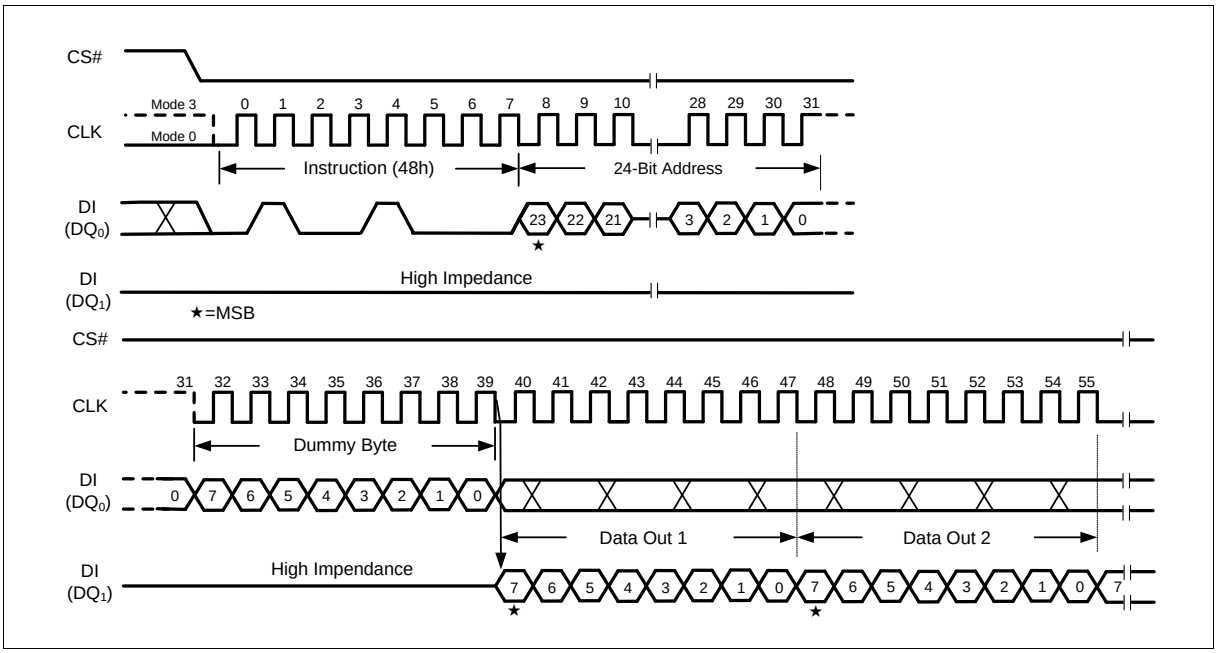


Figure 67 Read Security Sectors Command (SPI Mode only)

8.4.39 Set Read Parameters (C0h)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, “Set Read Parameters (C0h)” command can be used to configure the number of dummy clocks for “Fast Read (0Bh)”, “Fast Read Quad I/O (EBh)” & “Burst Read with Wrap (0Ch)” commands, and to configure the number of bytes of “Wrap Length” for the “Burst Read with Wrap (0Ch)” command.

In Standard SPI mode, the “Set Read Parameters (C0h)” command is not accepted. The dummy clocks for various Fast Read commands in Standard/Dual/Quad SPI mode are fixed, please refer to Table 24~Table 27 the Command set for details. The “Wrap Length” is set by W5-4 bit in the “Set Burst with Wrap (77h)” command. This setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

The default “Wrap Length” after a power up or a Reset command is 8 bytes, the default number of dummy clocks is 2.

P5 – P4	DUMMY CLOCKS	MAXIMUM READ FREQ.
0 0	2	50MHz
0 1	4	80MHz
1 0	6	104MHz
1 1	8	104MHz

P1 – P0	WRAP LENGTH
0 0	8-byte
0 1	16-byte
1 0	32-byte
1 1	64-byte

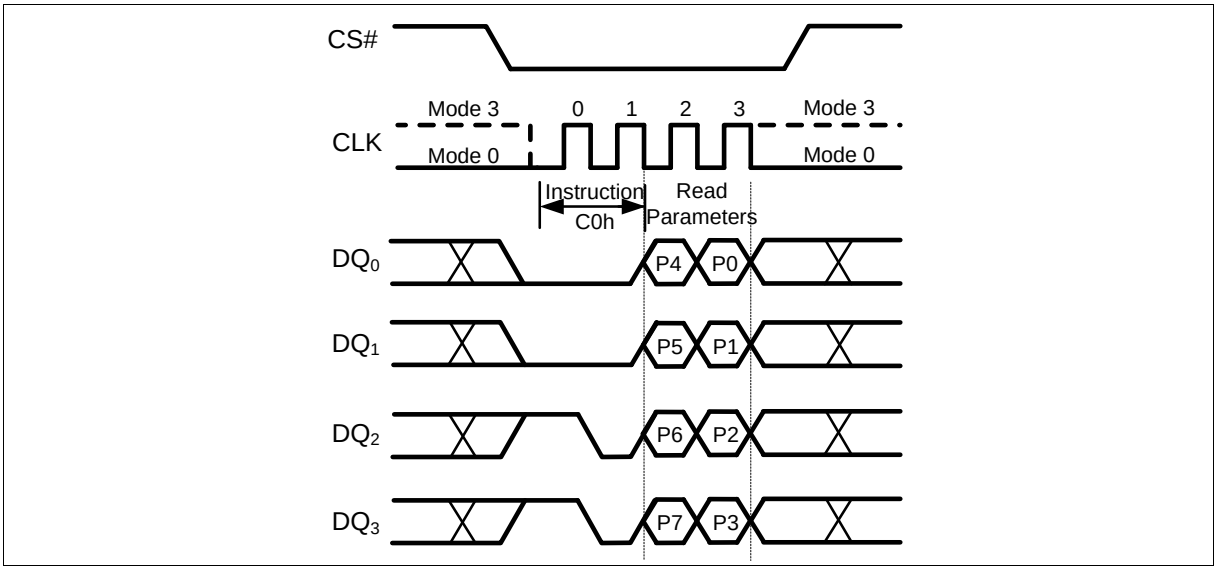


Figure 68 Set Read Parameters Command (QPI Mode only)

8.4.40 Burst Read with Wrap (0Ch)

The “Burst Read with Wrap (0Ch)” command provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The command is similar to the “Fast Read (0Bh)” command in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters C0h)” command.

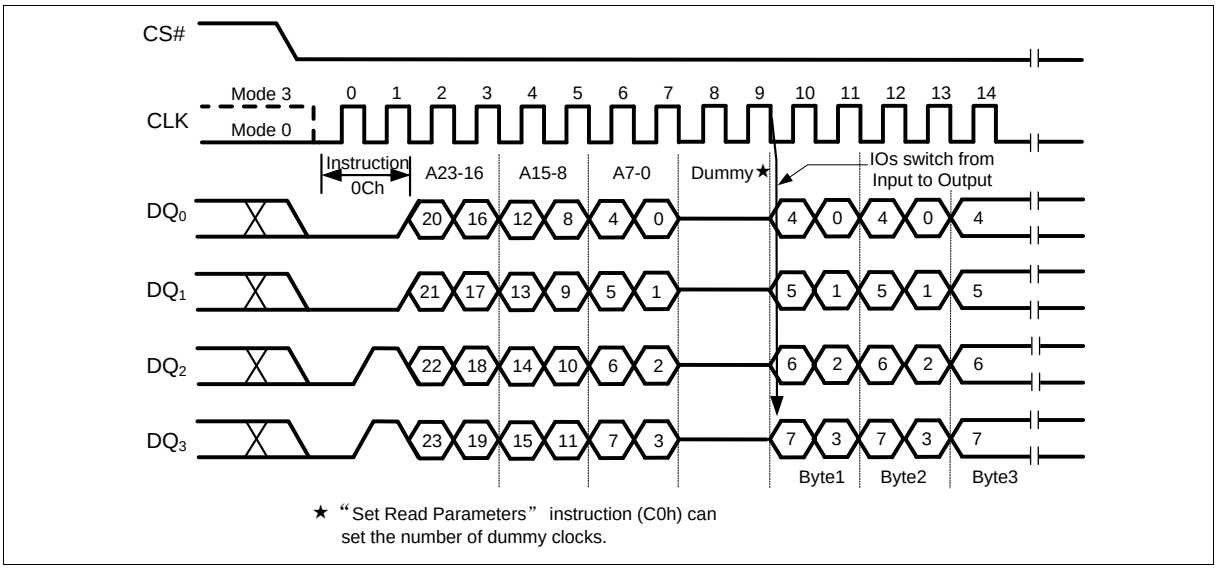


Figure 69 Burst Read with Wrap Command (QPI Mode only)

8.4.41 Individual Sector Lock(36h)

The Individual Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Sector Locks, the WPS bit in Status Register-3 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, SEC,TB, BP[2:0] bits in the Status Registers. The Individual Sector Lock bits are volatile bits. The default value after power up or after Reset are 1, so the entire memory array is being protected.

To lock a specific sector as illustrated in Figure 7, an Individual Sector Lock command must be issued by driving CS# low, shifting the command code “36h” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address and then driving CS# high.

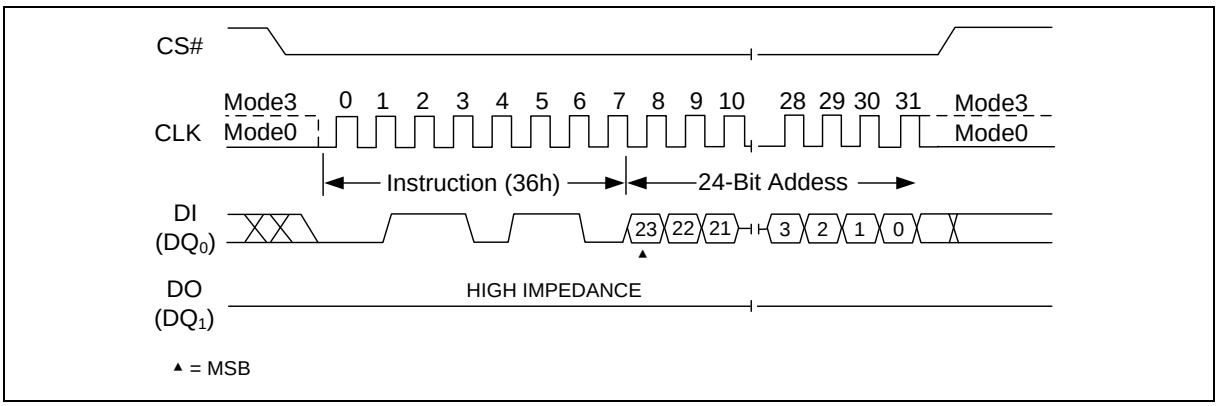


Figure 70 Read Sector Lock Command (SPI Mode only)

8.4.42 Individual Sector Unlock(39h)

The Individual Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Sector Locks, the WPS bit in Status Register-3 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, SEC,TB, BP[2:0] bits in the Status Registers. The Individual Sector Lock bits are volatile bits. The default value after power up or after Reset are 1, so the entire memory array is being protected.

To unlock a specific sector as illustrated in Figure 7, an Individual Sector Lock command must be issued by driving CS# low, shifting the command code “39h” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address and then driving CS# high.

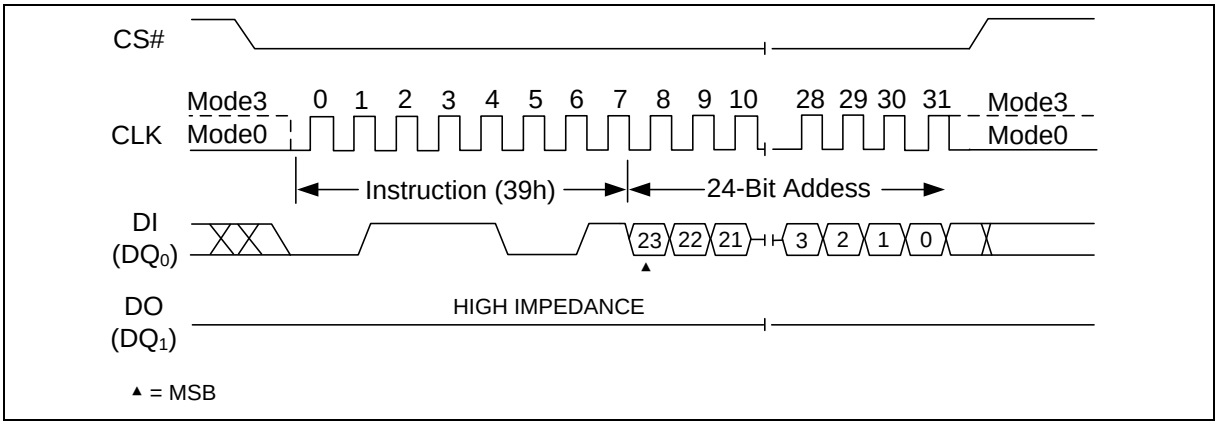


Figure 71 Individual Sector Lock Command (SPI Mode only)

8.4.43 Read Sector Lock (3Dh)

The Individual Sector Lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Sector Locks, the WPS bit in Status Register-3 must be set to 1. If WPS=0, the write protection will be determined by the combination of CMP, SEC,TB, BP[2:0] bits in the Status Registers. The Individual Sector Lock bits are volatile bits. The default value after power up or after Reset are 1, so the entire memory array is being protected.

To read out the lock bit of a specific sector as illustrated in Figure 7, an Read Sector Lock command must be issued by driving CS# low, shifting the command code “3Dh” into the Data Input (DI) pin on the rising edge of CLK, followed by a 24-bit address and then driving CS# high. The Sector Lock bit value will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) as shown in . If the least significant bit (LSB) is 1, the corresponding sector is locked; if LSB=0, the corresponding sector is unlocked, Erase/Program operation can be performed.

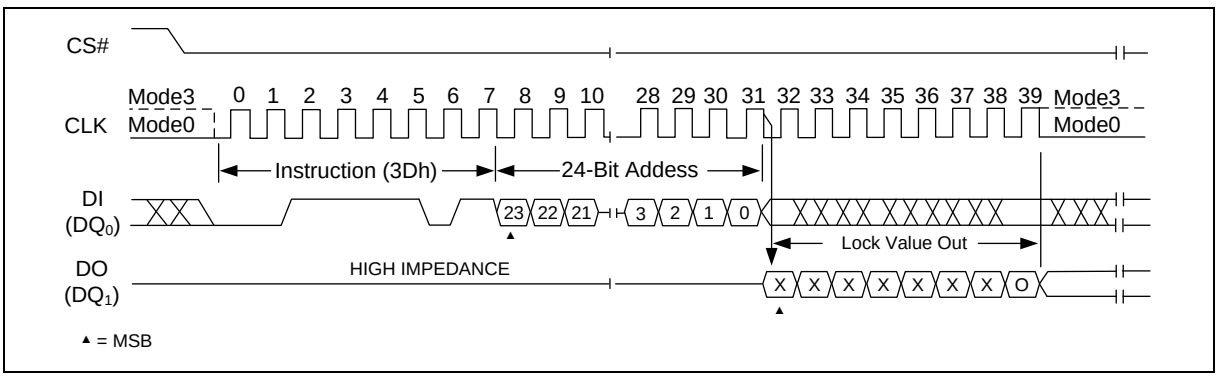


Figure 72 Read Sector Lock Command (SPI Mode only)

8.4.44 Global Sector Lock (7Eh)

All Sector Lock bits can be set to 1 by the Global Sector Lock command. The command must be issued by driving CS# low, shifting the command code “7Eh” into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

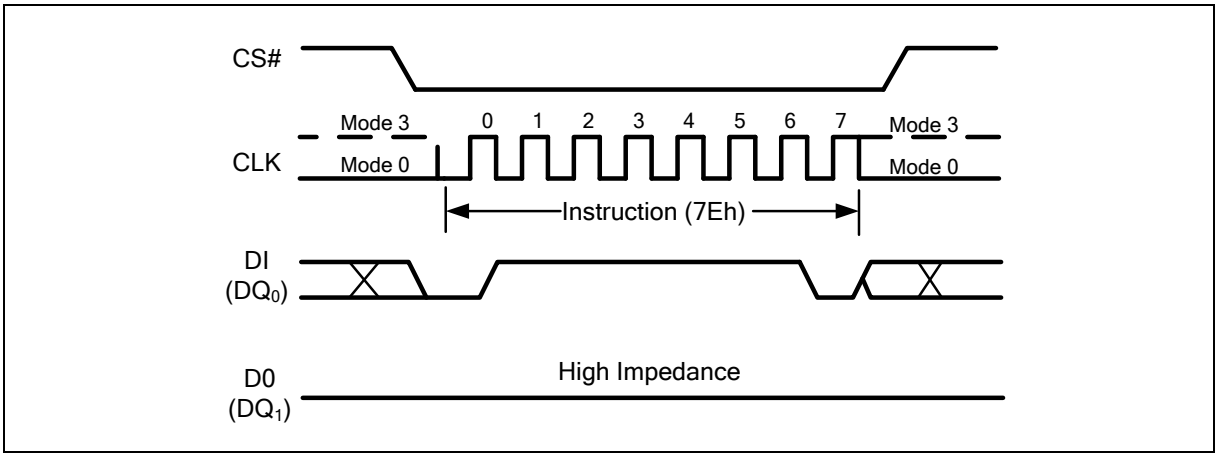


Figure 73 Global Sector Lock Command (SPI Mode only)

8.4.45 Global Sector Unlock (98h)

All Sector Lock bits can be set to 0 by the Global Sector Unlock command. The command must be issued by driving CS# low, shifting the command code “98h” into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

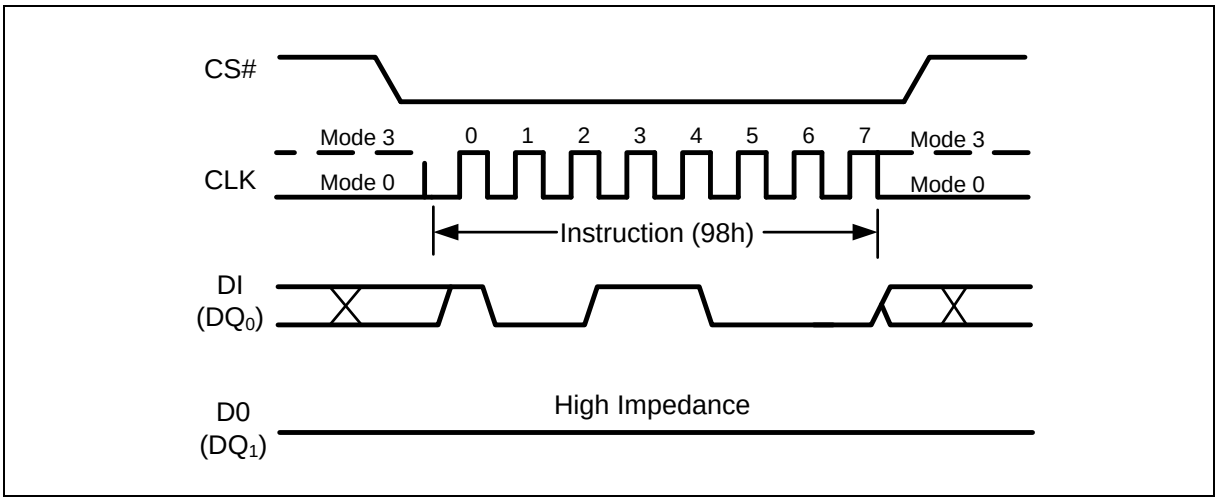


Figure 74 Global Sector Unlock Command (SPI Mode only)

8.4.46 Enable QPI (38h)

The FM25NQ04TX support both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode can not be used at the same time. “Enable QPI (38h)” command is the only way to switch the device from SPI mode to QPI mode.

Upon power-up, the default state of the device upon is Standard/Dual/Quad SPI mode. See Table 24~Table 26 Command Set for all supported SPI commands. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register 2 must be set to 1 first, and an “Enable QPI (38h)” command must be issued. If the Quad Enable (QE) bit is 0, the “Enable QPI (38h)”

command will be ignored and the device will remain in SPI mode.

See Table 27 Command Set for all the commands supported in QPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

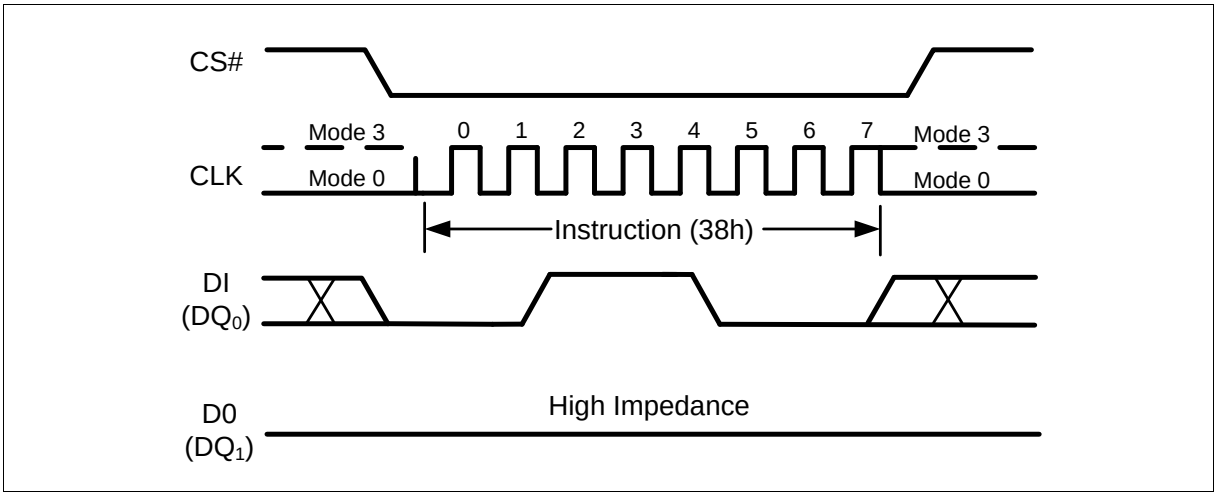


Figure 75 Enable QPI Command (SPI Mode only)

8.4.47 Disable QPI (FFh)

In order to exit the QPI mode and return to the Standard/Dual/Quad SPI mode, a “Disable QPI (FFh)” command must be issued.

When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status and the Wrap Length setting will remain unchanged.

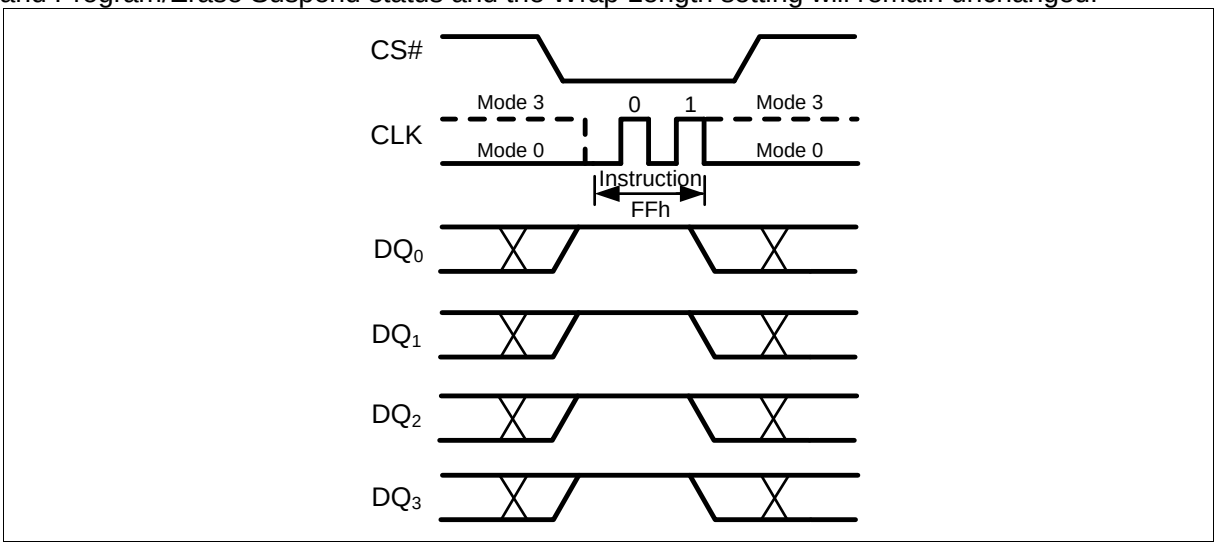


Figure 76 Disable QPI Command (QPI Mode only)

8.4.48 Enable Reset (66h) and Reset (99h)

Because of the small package and the limitation on the number of pins, the FM25NQ04TX provide a software Reset command instead of a dedicated RESET pin. Once the Reset command is accepted, any on-going internal operations will be terminated and the device will return to its

default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Read parameter setting P7-P0, Continuous Read Mode bit setting M7-M0 and Wrap Bit setting W6-W4.

"Enable Reset (66h)" and "Reset (99h)" commands can be issued in either SPI mode or QPI mode. To avoid accidental reset, both commands must be issued in sequence. Any other commands other than "Reset (99h)" after the "Enable Reset (66h)" command will disable the "Reset Enable" state. A new sequence of "Enable Reset (66h)" and "Reset (99h)" is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately t_{RST}=30μs to reset. During this period, no command will be accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the WIP bit and the SUS bit in Status Register before issuing the Reset command sequence.

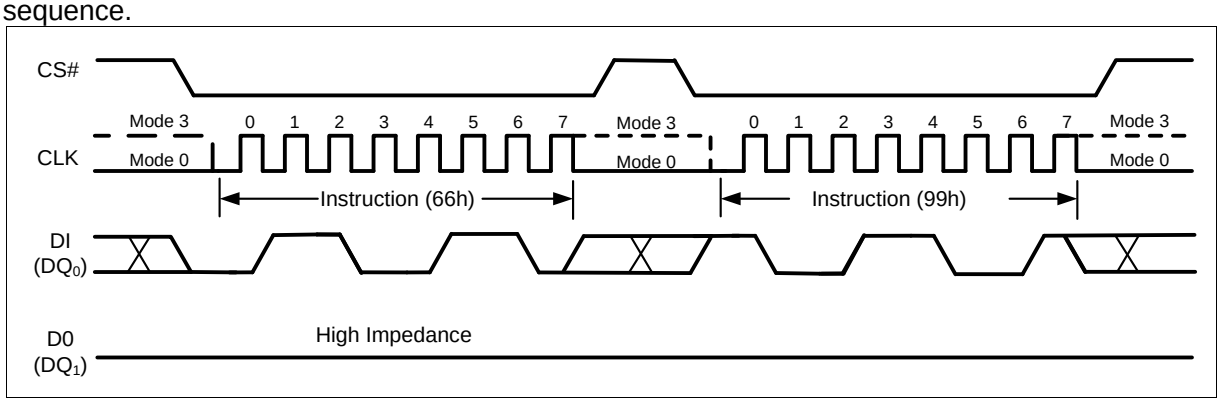


Figure 77 Enable Reset and Reset Command Sequence (SPI Mode)

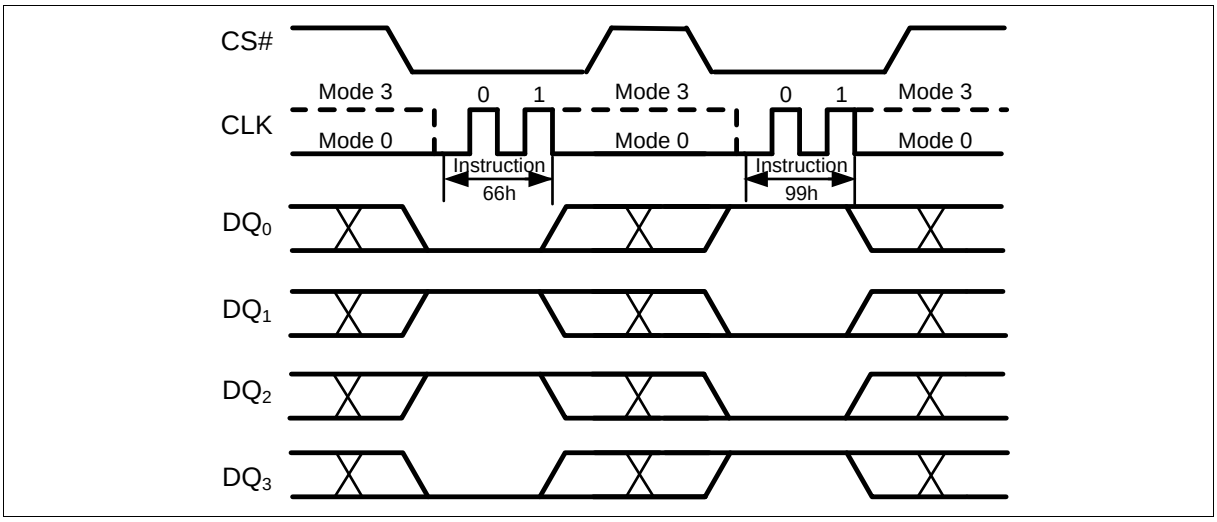


Figure 78 Enable Reset and Reset Command Sequence (QPI Mode)

8.4.49 Read Status Register-5 (RDSR5) (8Ah)

The Read Status Register 5 commands allow the Status Registers-5 to be read. The command is entered by driving CS# low and shifting the command code "8Ah" into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 79.

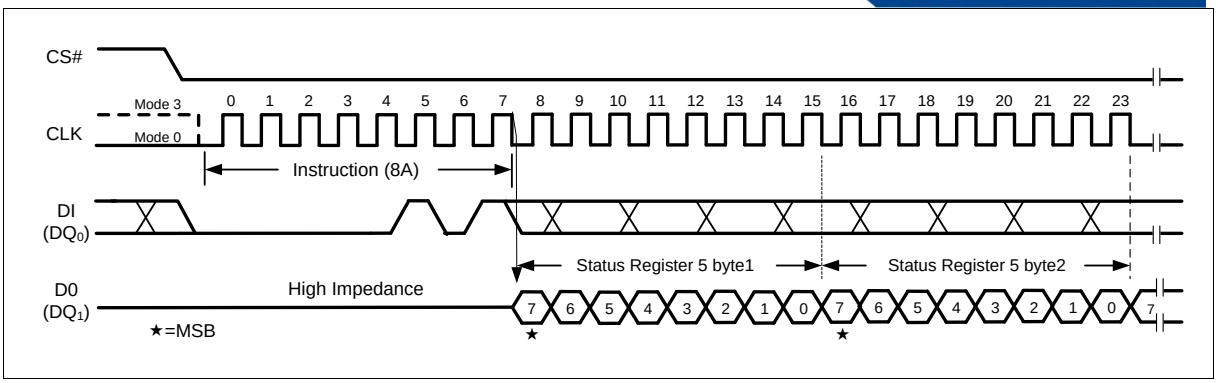


Figure 79 Read Status Register -5 Command (SPI Mode)

8.4.50 Write Status Register-5 (WRSR5) (88h)

The Write Status Register (WRSR) 5 command allows the Status Register 5 to be written. A CT_DATA_PWD authentication command must previously executed for the device to enter CT_DATA_PWD authenticated status. The command is entered by driving CS# low, sending the command code “88h”, and then writing the status register data byte as illustrated in Figure 18 and Figure 19.

To complete the Write Status Register (WRSR) command, the CS# pin must be driven high after the sixteenth bit of data that is clocked in. If this is not done the Write Status Register (WRSR) command will not be executed.

After CS# is driven high, the self-timed Write Status Register cycle will commence for a time duration of t_W (See “11.2.3 AC Characteristics”).

The Write Status Register-5 (WRSR5) command can be used only in SPI mode

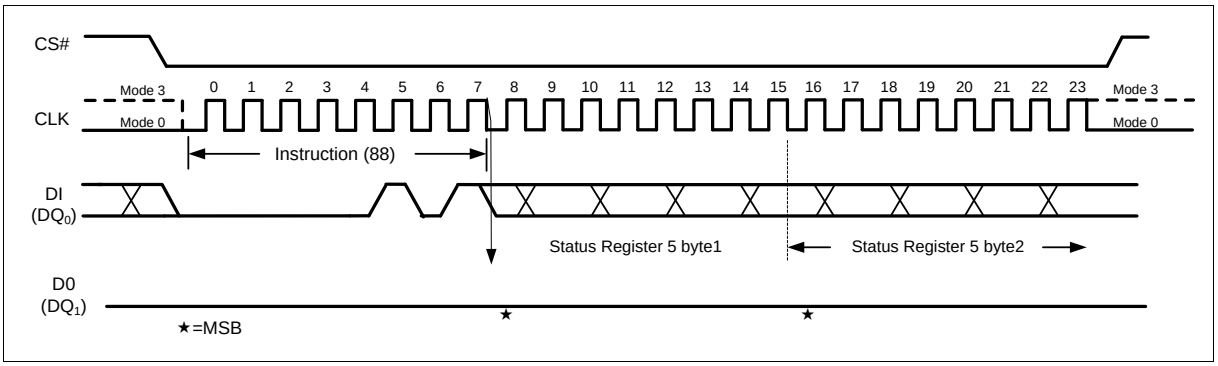


Figure 80 Write Status Register -5 Command (SPI Mode)

8.4.51 Data Password command

For write operation to status register 5, the device has two status, verified status in which status register 5 and password itself can be modified and unverified status in which status register 5 or password cannot be modified. The status is determined by password verification operation.

There are four password operations: password authentication, password write, password read and password de-authentication.

After power up, the device is in unverified status. A successful password verification operation makes the device enter verified status. In this status, password can be read or write. After a password verification disable command, the device returns to unverified status.

8.4.51.1 Password authentication

Password authentication operation must be performed in unauthenticated status. Otherwise, it is regarded as password write refer to section 8.4.51.2.

It is initiated by driving CS# low, sending the command code “89h”, following four bytes password. After driving CS# high, an internal comparison progress is triggered. The internal logic unit compares the 4 bytes input data and the 4 bytes password stored in memory. If the input data matches the password, the password authentication operation is successful and the device enters authenticated status. If the input data does not match password, the password authentication operation is fail and the device remains unauthenticated state.

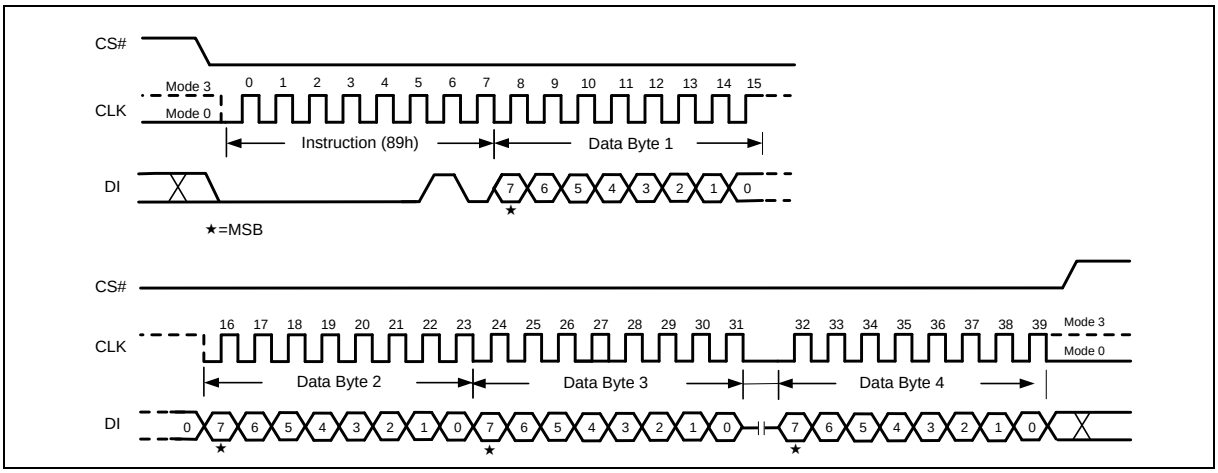


Figure 81 password authentication

8.4.51.2 Password write

Password write command is same as password authentication. If the device is already in authenticated status, this command will be regarded as password write command. After driving CS# high, internal write cycle is trigged and the password stored in memory is refreshed according to the input data.

8.4.51.3 Password read

In authenticated state, password can be read. It is initiated by driving CS# low, sending the command code “8Bh”, the password byte will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first.

After driving CS# high, the device returns to unauthenticated status.

If device receives password read command in unauthenticated status, the output data is all logic 0.

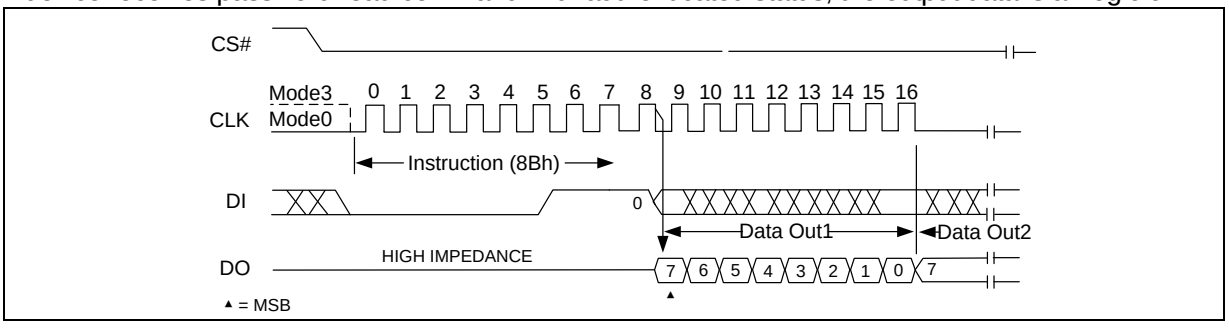


Figure 82 password read in authenticated state

8.4.51.4 Password de-authentication

After driving CS# high of password read command, the device returns to unauthenticated state.

8.5 TAG memory Command

8.5.1 TAG commands set

Command	Device Address	Address	Data
TAG memory Write	82h	0000h~00BFh for FM24NQ04T1 0000h~021Fh for FM24NQ04T2 0000h~039Fh for FM24NQ04T4 0000h~077Fh for FM24NQ04T4	1~16 bytes
TAG memory Read	86h	0000h~00BFh for FM24NQ04T1 0000h~021Fh for FM24NQ04T2 0000h~039Fh for FM24NQ04T4 0000h~077Fh for FM24NQ04T4	Output n bytes
TAG memory Password authentication	83h (un-authenticated state)		4 bytes PWD
TAG memory Password write	83h (authenticated state)		4 bytes new PWD
TAG memory Password read	87h (authenticated state)	-	Output 4 bytes PWD
TAG memory Password de-authentication	87h (authenticated state)	-	-
Tag Write enable	8Eh	-	-
Tag Write disable	8Fh	-	-
Read tag status register 1	84h	-	1 byte
Write tag status register 1	80h	-	1 byte
Read tag status register 2	85h	-	3 bytes
Write tag status register 2	81h	-	3 bytes
TAG UID read	8Ch		9 bytes

All tag commands are stand SPI commands.

8.5.2 TAG write (82h)

The write command allows from one byte to 16 bytes (a page) of data to be programmed at tag memory. A Tag Write Enable command must be executed before the device will accept the Write Command (Status Register bit WEL= 1). The command is initiated by driving the CS# pin low then shifting the command code “82h” followed by a 16-bit address A15-A0 and at least one data byte, into the DI pin. The CS# pin must be held low for the entire length of the command while data is being sent to the device. The write command sequence is shown in Figure 83.

If an entire 16 byte page is to be programmed, the last 4 address bits should be set to 0. If the last 4 address bits are not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 16 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 16 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase commands, the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the write command will not be executed. After CS#

is driven high, the self-timed write command will commence for a time duration of t_{wr} (See “11.2.3 AC Characteristics”). While the write cycle is in progress, the Read Status Register command may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the write cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The write command will not be executed if the addressed page is protected by the CT_TAG_WR_LOCK bit.

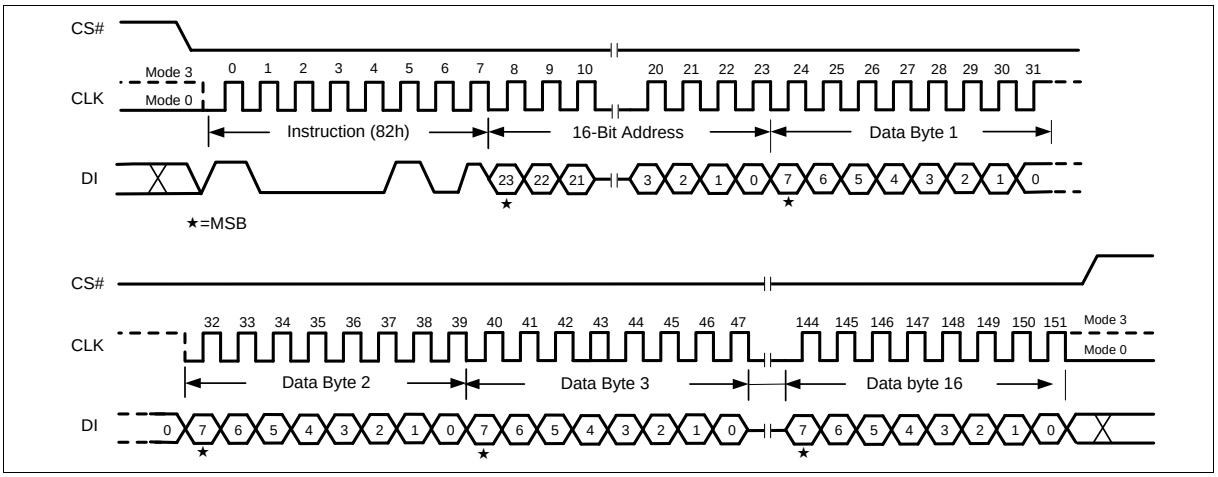


Figure 83 TAG Write Instruction

8.5.3 TAG read(86h)

The Read command allows one or more data bytes to be sequentially read from the TAG memory. The command is initiated by driving the CS# pin low and then shifting the command code “86h” followed by a 16-bit address A15-A0 into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single command as long as the clock continues. The command is completed by driving CS# high.

The Read Data command sequence is shown in Figure 22. If a Read Data command is issued while a Write cycle is in process (WIP =1) the command is ignored and will not have any effect on the current cycle. The Read Data command allows clock rates from D.C. to a maximum of f_R (see “11.2.3_AC Characteristics”).

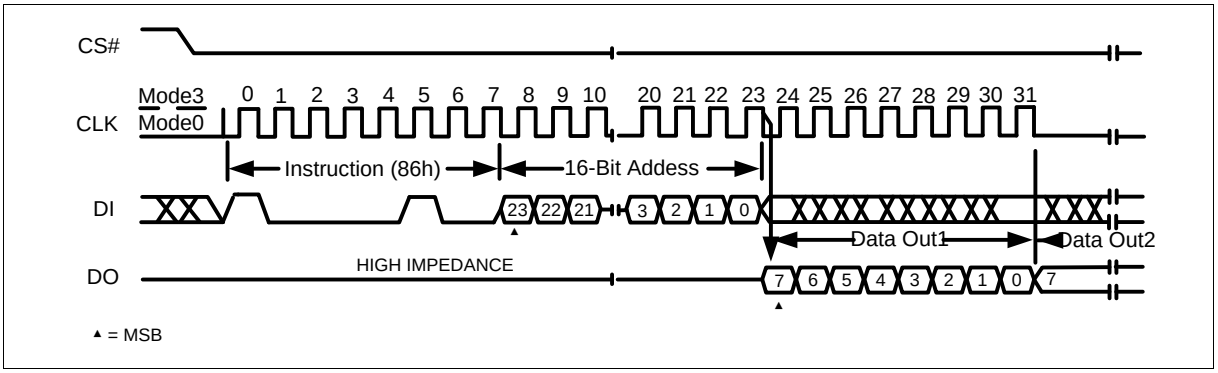


Figure 84 TAG Read Instruction

8.5.4 TAG Write enable(8Eh)

The Write Enable (WREN) instruction (Figure 85) sets the Write Enable Latch (WEL) bit in the TAG Status Register to a 1. The WEL bit must be set prior to every Tag Write and tag Write Status Register instruction. The Write Enable **(**WREN**)** instruction is entered by driving CS# low, shifting the instruction code “8Eh” into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

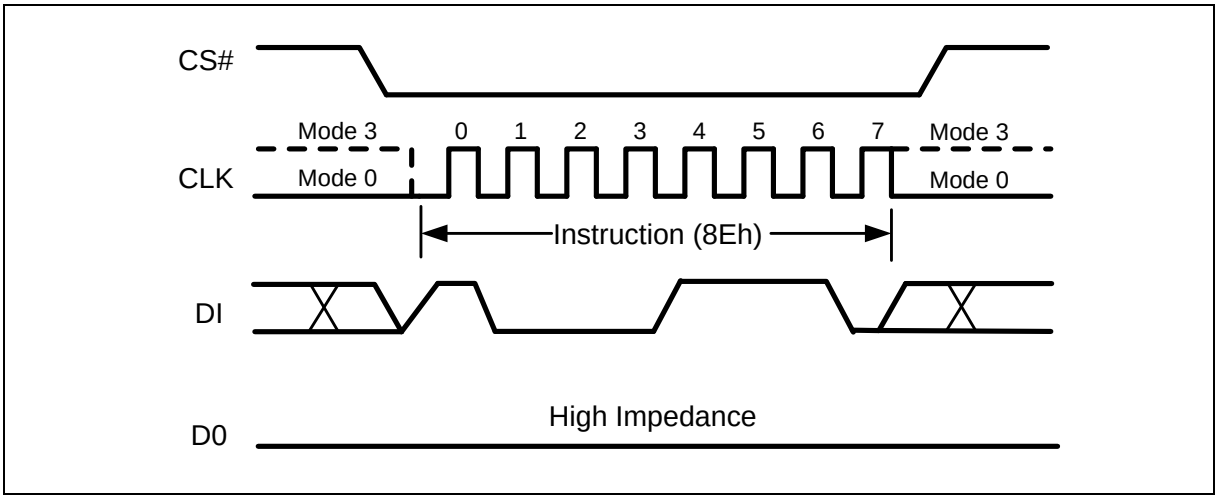


Figure 85 TAG Write enable Instruction

8.5.5 TAG Write disable(8Fh)

The Tag Write Disable (WRDI) instruction (Figure 86) resets the Write Enable Latch (WEL) bit in the Tag Status Register to a 0. The TAG Write Disable (WRDI) instruction is entered by driving CS# low, shifting the instruction code “8Fh” into the DI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Tag Write and tag Write Status Register instructions.

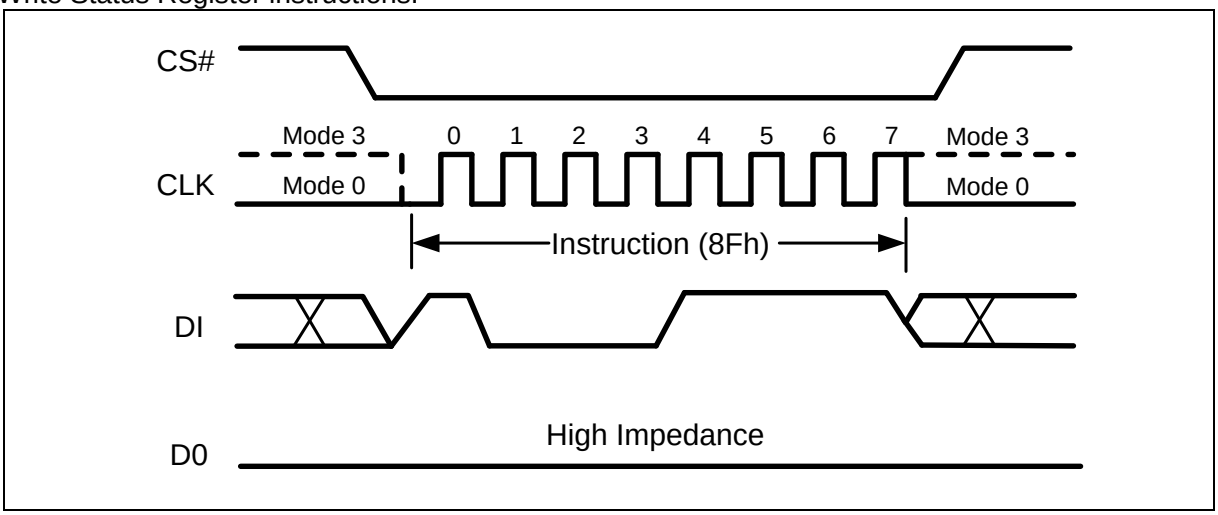


Figure 86 TAG Write disable Instruction

8.5.6 Read tag status register 1(84h)

The Read Tag Status Register 1 instruction allows the 8-bit TAG Status Registers 1 to be read. The instruction is entered by driving CS# low and shifting the instruction code “84h”. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 16. The Status Register bits are shown in Figure 9.

The Read Tag Status Register instruction may be used at any time. When this instruction is used while a Write cycle to tag memory is in progress or tag memory being accessed by RF interface, the CT_TAG_WR_LOCK bit is always 0 and the WIP and WEL bits make sense. This allows the WIP status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 87. The instruction is completed by driving CS# high.

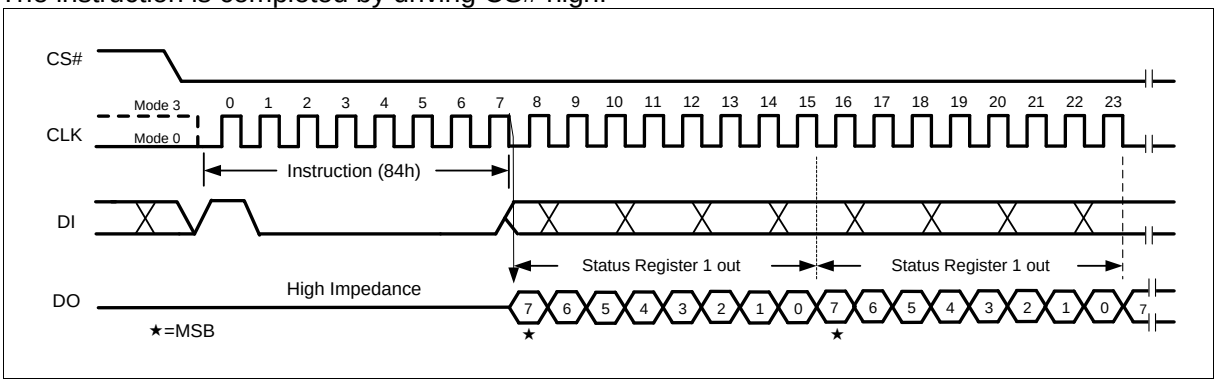


Figure 87 Read tag status register 1 Instruction

8.5.7 Read tag status register 2(85h)

The Read Tag Status Register 2 instruction allows the 24-bit TAG Status Registers 2 to be read. The instruction is entered by driving CS# low and shifting the instruction code “85h”. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure 88. The Status Register bits are shown in Figure 10.

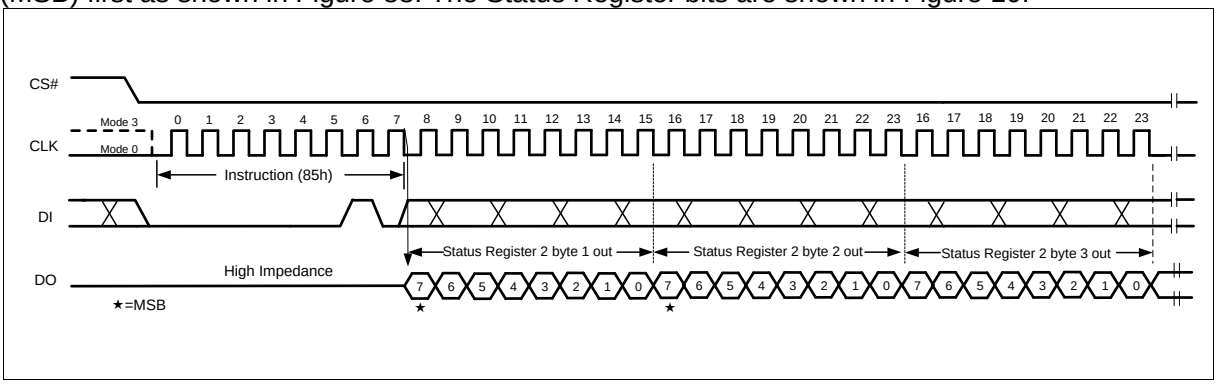


Figure 88 Read tag status register 2 Instruction

8.5.8 Write Tag Status Register-1 (80h)

The Write Tag Status Register (WRSR) 1 command allows the Tag Status Register 1 to be written. A CT_TAG_PWD authentication command and a TAG Write Enable command must previously executed. The command is entered by driving CS# low, sending the command code “80h”, and then writing the status register data byte as illustrated in Figure 89. Only the non-volatile bits can be written.

To complete the Write Status Register (WRSR) command, the CS# pin must be driven high after the eighth bit of data that is clocked in. If this is not done the Write Status Register (WRSR) command will not be executed.

After CS# is driven high, the self-timed Write Status Register cycle will commence for a time duration of t_W (See “11.2.3 AC Characteristics”).

The Write Status Register (WRSR) command can be used only in SPI mode.

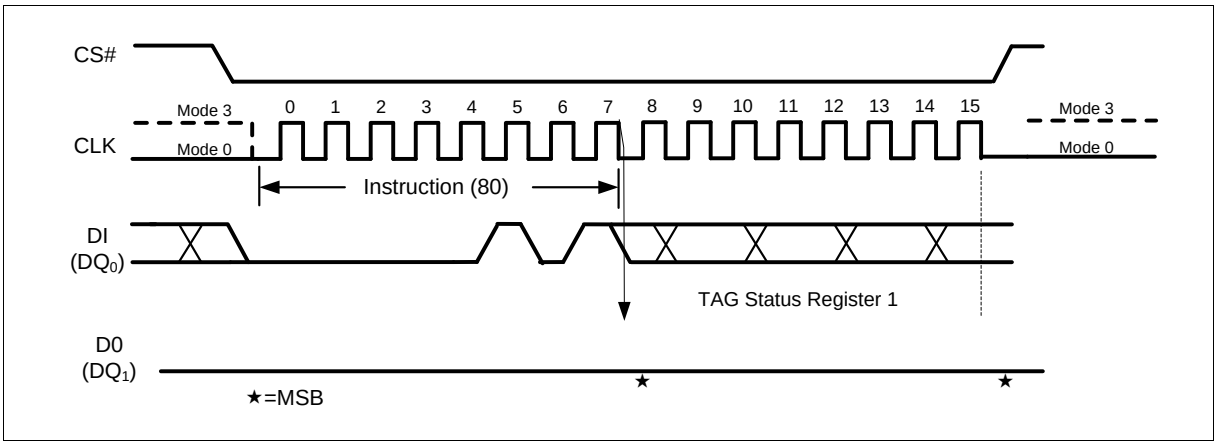


Figure 89 Write tag status register 1 Instruction

8.5.9 Write Tag Status Register-2 (81h)

The Write Tag Status Register (WRSR) 2 command allows the Tag Status Register 2 to be written. A CT_TAG_PWD authentication command and a TAG Write Enable command must previously executed. The command is entered by driving CS# low, sending the command code “81h”, and then writing the status register data byte as illustrated in Figure 90.

To complete the Write Status Register (WRSR) command, the CS# pin must be driven high after the twenty-fourth bit of data that is clocked in. If this is not done the Write Status Register (WRSR) command will not be executed.

After CS# is driven high, the self-timed Write Status Register cycle will commence for a time duration of t_W (See “11.2.3 AC Characteristics”).

The Write Status Register (WRSR) command can be used only in SPI mode.

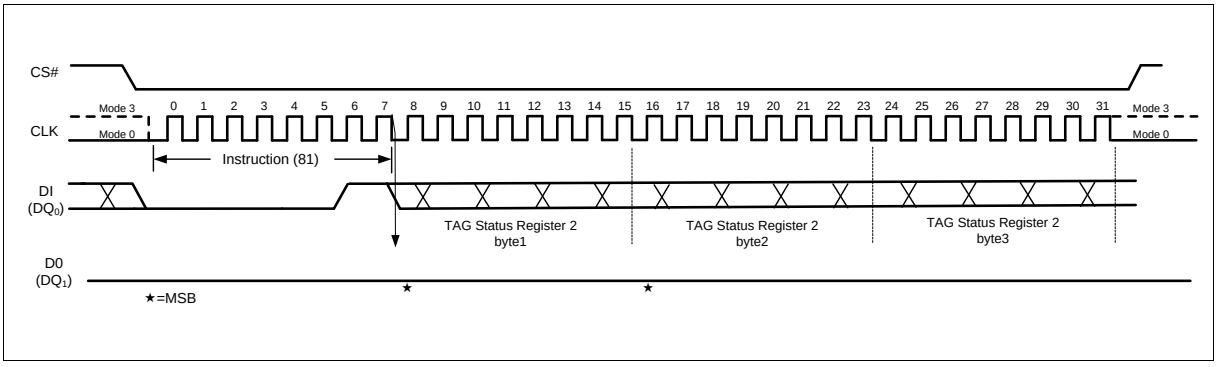


Figure 90 Write tag status register 2 Instruction

8.5.10 TAG Password command

For write operation to tag memory, the device has two status, verified status in which tag status register and password itself can be modified using write status register command and unverified status in which status register and password cannot be modified. The status is determined by password verification operation.

There are four password operations: password authentication, password write, password read

and password de-authentication.

After power up, the device is in unverified status. A successful password authentication operation makes the device enter verified status. After a password de-authentication command, the device returns to unverified status.

The 4 bytes password is stored in memory with default value all 00h. The password can be read out in authenticated status.

8.5.10.1 Password authentication (83h)

Password authentication operation must be performed in unauthenticated status. Otherwise, it is regarded as password write refer to section 8.5.10.2.

It is initiated by driving CS# low, sending the command code “83h”, following four bytes password. After driving CS# high, an internal comparison progress is triggered. The internal logic unit compares the 4 bytes input data and the 4 bytes password stored in memory. If the input data matches the password, the password authentication operation is successful and the device enters authenticated status. If the input data does not match password, the password authentication operation is fail and the device remains unauthenticated state.

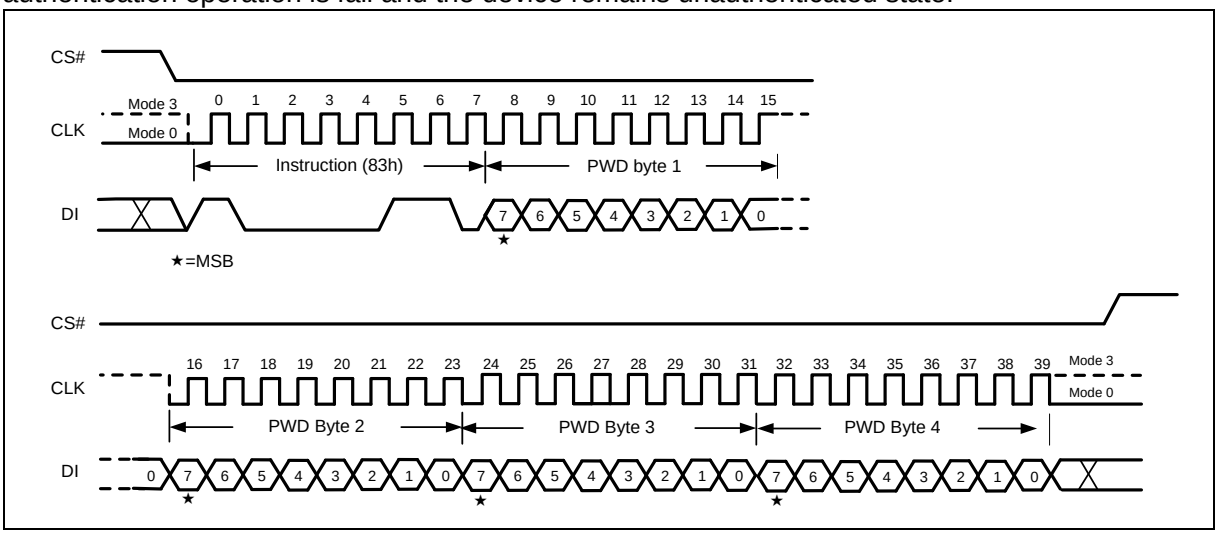


Figure 91 Password authentication

8.5.10.2 Password write (83h)

Password write command is same as password authentication. If the device is already in authenticated status, this command will be regarded as password write command. After driving CS# high, internal write cycle is trigged and the password stored in memory is refreshed according to the input data.

8.5.10.3 Password read (87h)

In authenticated state, password can be read. It is initiated by driving CS# low, sending the command code “87h”, the password byte will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first.

After driving CS# high, the device returns to unauthenticated status.

If device receives password read command in unauthenticated status, the output data is all logic 0.

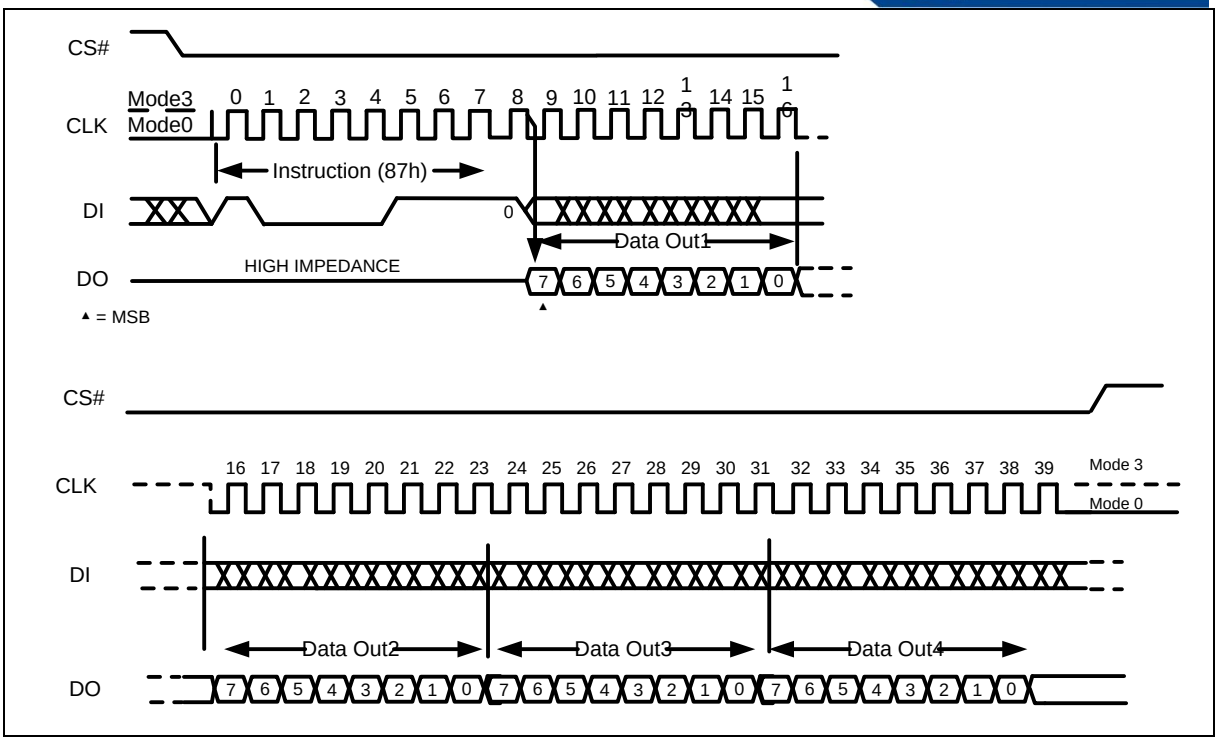


Figure 92 Password read in authenticated state

8.5.10.4 Password de-authentication (87h)

After driving CS# high of password read command, the device returns to unauthenticated state.

9 RF interface

The RF-interface is based on the ISO/IEC 14443 Type A standard.

During operation, the NFC device generates an RF field. The RF field must always be present (with short pauses for data communication) as it is used for both communication and as power supply for the Digital Control Unit of tag. During RF interface operation, contact power supply pin (VCC) must be power on, because the power of EEPROM memory is supplied by Vcc pin. The harvested energy of EH_FD pin comes from RF field.

For both directions of data communication, there is one start bit at the beginning of each frame. Each byte is transmitted with an odd parity bit at the end. The LSB of the byte with the lowest address of the selected block is transmitted first. The maximum length of a NFC device to FM25NQ04Tx frame is 2369 bits (1 PCB byte + 1 INS byte + 2 address bytes + 1 Lc byte + 256 data bytes + 2 CRC bytes + 1 start bit). The maximum length of a FM25NQ04Tx to NFC device frame is 2326 bits (256 data bytes + 2 CRC bytes + 1 start bit). The TAG FAST_READ command has a variable frame length depending on the start and end address parameters. The maximum frame length supported by the NFC device needs to be taken into account when issuing this command.

For a multi-byte parameter, the least significant byte is always transmitted first. As an example, when reading from the tag memory using the READ command, byte 0 from the addressed block is transmitted first, followed by byte 1 to byte 3 out of this block. The same sequence continues for the next block and all subsequent blocks.

9.1 Communication principle

The commands are initiated by the NFC device and controlled by the Digital Control Unit of the FM25NQ04Tx. The command response is depending on the state of the IC and for memory operations also on the access conditions valid for the corresponding page.

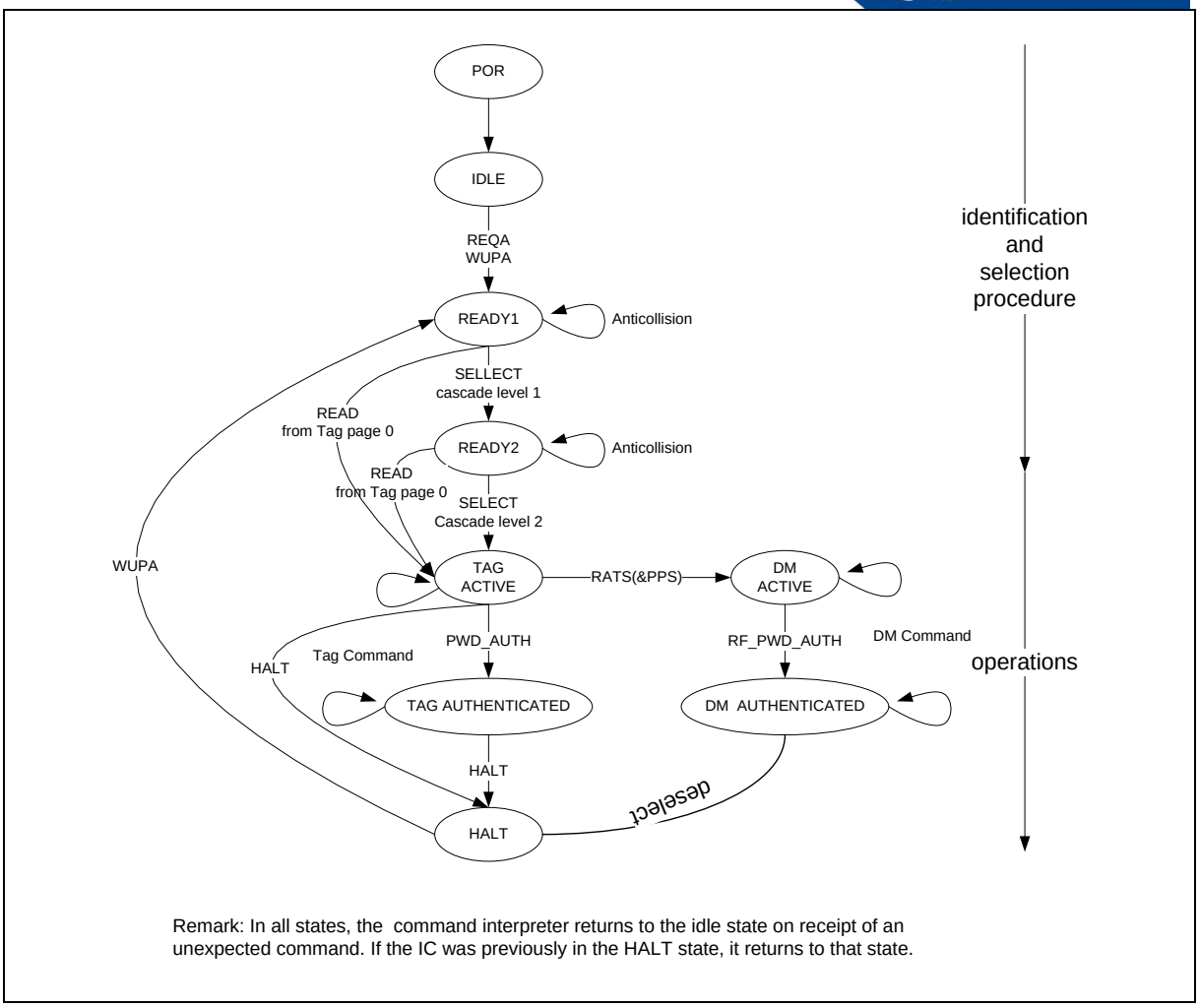


Figure 93 state diagram of RF interface

9.1.1 IDLE state

After a power-on reset (POR), FM25NQ04Tx switches to the IDLE state. It only exits this state when a REQA or a WUPA command is received from the NFC device. Any other data received while in this state is interpreted as an error and FM25NQ04Tx remains in the IDLE state.

After a correctly executed HLTA command i.e. out of the ACTIVE or AUTHENTICATED state, the default waiting state changes from the IDLE state to the HALT state. This state can then be exited with a WUPA command only.

9.1.2 READY1 state

In this state, the NFC device resolves the first part of the UID (3 bytes) using the ANTICOLLISION or SELECT commands in cascade level 1. This state is correctly exited after execution of either of the following commands:

• SELECT command from cascade level 1: the NFC device switches FM25NQ04Tx into READY2 state where the second part of the UID is resolved.

• READ command (from address 0): all anticollision mechanisms are bypassed and the FM25NQ04Tx switches directly to the ACTIVE state.

Remark: If more than one tag is in the NFC device field, a READ command from address 0 selects all FM25NQ04Tx devices. In this case, a collision occurs due to different serial numbers.

Any other data received in the READY1 state is interpreted as an error and depending on its previous state FM25NQ04Tx returns to the IDLE or HALT state.

9.1.3 READY2 state

In this state, FM25NQ04Tx supports the NFC device in resolving the second part of its UID (4 bytes) with the cascade level 2 ANTICOLLISION command. This state is usually exited using the cascade level 2 SELECT command.

Alternatively, READY2 state can be skipped using a READ command (from address 0) as described for the READY1 state.

Remark: The response of FM25NQ04Tx to the cascade level-2 SELECT command is the Select Acknowledge (SAK) byte. In accordance with ISO/IEC 14443, this byte indicates if the anticollision cascade procedure has finished. FM25NQ04Tx is now uniquely selected and only this device will communicate with the NFC device even when other contactless devices are present in the NFC device field. If more than one FM25NQ04Tx is in the NFC device field, a READ command from address 0 selects all FM25NQ04Tx devices. In this case, a collision occurs due to the different serial numbers. Any other data received when the device is in this state is interpreted as an error. Depending on its previous state the FM25NQ04Tx returns to either the IDLE state or HALT state.

9.1.4 TAG ACTIVE state

All tag operations and other functions like the originality check are operated in this state.

The ACTIVE state is exited with the HLTA command and upon reception FM25NQ04Tx transits to the HALT state. Any other data received when the device is in this state is interpreted as an error. Depending on its previous state, FM25NQ04Tx returns to either the IDLE state or HALT state.

FM25NQ04Tx transits to the TAG AUTHENTICATED state after successful password verification using the PWD_AUTH command.

9.1.5 TAG AUTHENTICATED state

In this state, all operations on TAG memory blocks, which are configured as password verification protected, can be accessed.

The TAG AUTHENTICATED state is exited with the HLTA command and upon reception FM25NQ04Tx transits to the HALT state. Any other data received when the device is in this state is interpreted as an error. Depending on its previous state, FM25NQ04Tx returns to either the IDLE state or HALT state.

9.1.6 Data Memory (DM) ACTIVE state

In this state, data memory can be read and authentication can be performed. Any write command to data memory is not permitted.

Any other data received when the device is in this state is interpreted as an error and FM24NCQ04Tx returns to HALT state.

FM24NCQ04Tx transits to the DM AUTHENTICATED state after successful RF password verification using the RF_PWD_AUTH command.

9.1.7 Data Memory (DM) AUTHENTICATED state

In this state, all operations on RF read/write data memory and lock bits can be accessed.

Any other data received when the device is in this state is interpreted as an error and FM24NCQ04Tx returns to HALT state.

9.1.8 HALT state

HALT and IDLE states constitute the two wait states implemented in FM25NQ04Tx. An already processed FM25NQ04Tx can be set into the HALT state using the HLTA or deselect command. In the anti-collision phase, this state helps the NFC device to distinguish between processed tags and tags yet to be selected. FM25NQ04Tx can only exit this state on execution of the WUPA command. Any other data received when the device is in this state is interpreted as an error and FM25NQ04Tx state remains unchanged.

9.2 RF operation

9.2.1 Data operation

9.2.1.1 Tag Memory Operation

Using RF tag memory command, RF interface can access tag memory. Tag memory command can see section 9.3.2. These commands are used to read or write data in tag memory.

9.2.1.2 Data Memory Operation

Using RF data memory command, RF interface can access 4Mbit data memory. Data memory command includes READ, PP, SE, BE32, BE64, RDSR1/2/3/4/5, WRSR1/2/3/4/5, WREN, WRDI. The number of data bytes for READ and PP command can be configured, using 1 Lc byte for PP and 1 Le byte for READ, respectively. That is, 1~256 bytes can be transferred in the two commands. For other commands, the data byte is unnecessary or fixed.

Writing access of data memory in RF interface could be restricted by write protect mechanism defined in data memory status register, RF_DATA_WR_LOCK or Data memory unauthenticated status.

Reading access of data memory in RF interface could be restricted by RF_DATA_RD_LOCK.

9.2.1.3 Data Memory Lock Operation

Using RF lock command, the read and writing access in RF interface could be read and changed.

READ_RF_DATA_RD_LOCK and READ_RF_DATA_WR_LOCK commands are used to read RF_DATA_RD_LOCK and RF_DATA_WR_LOCK register individually. These two commands doesn't need RF_PWD authentication. They can operate not only in DM ACTIVE state, but also in DM AUTHENTICATED state.

WRITE_RF_DATA_RD_LOCK and WRITE_RF_DATA_WR_LOCK commands are used to Lock RF_DATA_RD_LOCK and RF_DATA_WR_LOCK individually. These two commands need RF_PWD authentication. They can operate only in DM AUTHENTICATED state.

WRITE_RF_DATA_RD_LOCK and WRITE_RF_DATA_WR_LOCK commands are bit-wise OR'ed. It can change lock bit to logic 1, but cannot change back to logic 0.

9.2.2 Data integrity

Following mechanisms are implemented in the contactless communication link between NFC device and FM25NQ04Tx to ensure very reliable data transmission:

- 16 bits CRC per block
- parity bits for each byte
- bit count checking
- bit coding to distinguish between "1", "0" and "no information"
- channel monitoring (protocol sequence and bit stream analysis)

9.2.3 ASCII mirror function

FM25NQ04Tx features a ASCII mirror function. This function enables FM25NQ04Tx to virtually mirror

- 7 byte UID
- 3 byte NFC counter value
- both, 7 byte UID and 3 byte NFC counter value with a sepration byte

into the physical tag memory of the IC. On the READ or FAST READ command to the involved user memory blocks, FM25NQ04Tx will respond with the virtual memory content of the UID in ASCII code.

The required length of the reserved physical memory for the mirror functions is specified as below.

- UID mirror 14 bytes
- NFC counter mirror 6 bytes
- UID + counter mirror 21 bytes (14 bytes UID + 1 byte separation + 6 byte counter)

The position within the user memory where the mirroring of the UID shall start is defined by the MIRROR_BLOCK and MIRROR_BYTE values.

The MIRROR_BLOCK value defines the block where the UID ASCII mirror shall start and the MIRROR_BYTE value defines the starting byte within the defined block.

9.2.3.1 UID ASCII mirror function

This function enables FM25NQ04Tx to virtually mirror the 7 byte UID in ASCII code into the physical memory of the IC. The length of the UID ASCII mirror requires 14 bytes to mirror the UID in ASCII code. On the READ or FAST READ command to the involved user memory blocks, FM24NQ04Tx will respond with the virtual memory content of the UID in ASCII code.

The position within the user memory where the mirroring of the UID shall start is defined by the MIRROR_BLOCK and MIRROR_BYTE values.

The MIRROR_BLOCK value defines the block where the UID ASCII mirror shall start and the MIRROR_BYTE value defines the starting byte within the defined block.

The UID ASCII mirror function is enabled with a MIRROR_BLOCK value >03h and the MIRROR_CONF bits are set to 01b.

Remark: Please note that the 14 bytes of the UID ASCII mirror shall not exceed the boundary of the tag user memory. Therefore it is required to use only valid values for MIRROR_BYTE and MIRROR_BLOCK to ensure a proper functionality.

Table 28 Configuration parameter descriptions

	MIRROR_BLOCK	MIRROR_BYTE bits
Minimum values	04h	00 - 11b
Maximum values	last user memory block - 3	10b

9.2.3.2 NFC counter mirror function

This function enables FM25NQ04Tx to virtually mirror the 3 byte NFC counter value in ASCII code into the physical memory of the IC. The length of the NFC counter mirror requires 6 bytes to mirror the NFC counter value in ASCII code. On the READ or FAST READ command to the involved user memory blocks, FM24NQ04Tx will respond with the virtual memory content of the NFC counter in ASCII code.

The position within the user memory where the mirroring of the NFC counter shall start is defined by the MIRROR_BLOCK and MIRROR_BYTE values.

The MIRROR_BLOCK value defines the block where the NFC counter mirror shall start and the

MIRROR_BYTE value defines the starting byte within the defined block.

The NFC counter mirror function is enabled with a MIRROR_BLOCK and MIRROR_BYTE value according to Table 29 and the MIRROR_CONF bits are set to 10b.

If the NFC counter is password protected with the NFC_CNT_PWD_PROT bit set to 1b (see 7.3.7), the NFC counter will only be mirrored into the physical memory, if avalid password authentication has been executed before.

The NFC counter ASCII mirror function is enabled with a MIRROR_BLOCK value >03h and the MIRROR_CONF bits are set to 10b.

Remark: Please note that the 6 bytes of the NFC counter mirror shall not exceed the boundary of the tag user memory. Therefore it is required to use only valid values for MIRROR_BYTE and MIRROR_BLOCK to ensure a proper functionality.

Table 29 Configuration parameter descriptions

	MIRROR_BLOCK	MIRROR_BYTE bits
Minimum values	04h	00 - 11b
Maximum values	last user memory block - 1	10b

9.2.3.3 UID and NFC counter mirror function

This function enables FM25NQ04Tx to virtually mirror the 7 byte UID and 3byte NFC counter value in ASCII code into the physical memory of the IC separated by 1 byte (“x” character, 78h). The length of the mirror requires 21 bytes to mirror the UID, NFC counter value and the separation byte in ASCII code. On the READ or FAST READ command to the involved user memory blocks, FM24NQ04Tx will respond with the virtual memory content of the UID and NFC counter in ASCII code.

The position within the user memory where the mirroring shall start is defined by the MIRROR_BLOCK and MIRROR_BYTE values.

The MIRROR_BLOCK value defines the block where the mirror shall start and the MIRROR_BYTE value defines the starting byte within the defined block.

The UID and NFC counter mirror function is enabled with a MIRROR_BLOCK and a MIRROR_BYTE value according to Table 30 and the MIRROR_CONF bits are set to 11b.

If the NFC counter is password protected with the NFC_CNT_PWD_PROT bit set to 1b (see 7.3.7), the NFC counter will only be mirrored into the physical memory, if a valid password authentication has been executed before.

The UID and NFC counter ASCII mirror function is enabled with a MIRROR_BLOCK value >03h and the MIRROR_CONF bits are set to 11b.

Remark: Please note that the 21 bytes of the UID and NFC counter mirror shall not exceed the boundary of the tag user memory. Therefore it is required to use only valid values for MIRROR_BYTE and MIRROR_BLOCK to ensure a proper functionality.

Table 30 Configuration parameter descriptions

	MIRROR_BLOCK	MIRROR_BYTE bits
Minimum values	04h	00 - 11b
Maximum values	last user memory block - 5	10b

9.2.4 RF tag Password verification protection

The memory write or read/write access to a configurable part of the tag memory by RF interface can be constrained to a positive password verification. The 32-bit secret password (PWD) and the 16-bit password acknowledge (PACK) responses are typically programmed into the configuration blocks at the tag personalization stage. The AUTHLIM parameter specified in Section 7.3.7 can be used to limit the negative verification attempts.

In the initial state of FM25NQ04Tx, password protection is disabled by a AUTH0 value of FFh. PWD and PACK are freely writable in this state. Access to the configuration blocks and any part of the user memory can be restricted by setting AUTH0 to a block address within the available memory space. This block address is the first one protected.

Remark: The password protection method provided in FM25NQ04Tx has to be intended as an easy and convenient way to prevent unauthorized memory accesses. If a higher level of protection is required, cryptographic methods can be implemented at application layer to increase overall system security.

9.2.4.1 Programming of Tag PWD and PACK

The 32-bit PWD and the 16-bit PACK need to be programmed into the configuration pages, see Section 7.3.7. The password as well as the password acknowledge are written LSByte first. This byte order is the same as the byte order used during the PWD_AUTH command and its response.

The PWD and PACK bytes can never be read out of the memory. Instead of transmitting the real value on any valid READ or FAST_READ command, only 00h bytes are replied.

If the password verification does not protect the configuration pages, PWD and PACK can be written with normal WRITE and COMPATIBILITY_WRITE commands.

If the configuration blocks are protected by the password configuration, PWD and PACK can be written after a successful PWD_AUTH command.

The PWD and PACK are writable even if the CFGLCK bit is set to 1b. Therefore it is strongly recommended to set AUTH0 to the block where the PWD is located after the password has been written. This block is 2Bh for FM25NQ04T1, 85h for FM25NQ04T2 and E5h for FM25NQ04T3.

Remark: To improve the overall system security, it is advisable to diversify the password and the password acknowledge using a die individual parameter, that is the 7-byte UID available on FM25NQ04Tx.

9.2.4.2 Limiting negative verification attempts

To prevent brute-force attacks on the password, the maximum allowed number of negative password verification attempts can be set using AUTHLIM. This mechanism is disabled by setting AUTHLIM to a value of 000b, which is also the initial state of FM25NQ04Tx.

If AUTHLIM is not equal to 000b, each of negative verification is internally counted. As soon as this internal counter reaches the number specified in AUTHLIM, any further negative password verification leads to a permanent locking of the protected part of the memory for the specified access modes. Specifically, whether the provided password is correct or not, each subsequent PWD_AUTH fails. Any successful password verification, before reaching the limit of negative password verification attempts, resets the internal counter to zero.

9.2.4.3 Protection of special memory segments

The configuration blocks can be protected by the password authentication as well. The protection level is defined with the PROT bit.The protection is enabled by setting the AUTH0 byte to a value that is within the addressable memory space.

9.2.5 Originality signature

FM25NQ04Tx features a cryptographically supported originality check. With this feature, it is possible to verify with a certain confidence that the tag is using an IC manufactured by Fudan microelectronics. This check can be performed on personalized tags as well. If you need further information, please contact us.

9.3 Command

9.3.1 Overview

NFC tag of FM25NQ04Tx activation follows the ISO/IEC 14443 Type A. After tag has been selected, it can either be deactivated using the ISO/IEC 14443 HLTA command, or the NFC tag commands (e.g. READ or WRITE) can be performed.

In RF interface command, the LSB of the byte is transmitted first.

9.3.1.1 Command Set

All available commands for FM25NQ04Tx are shown in Table 31.

Table 31 FM25NQ04Tx RF Command Set

Command category	Command	ISO/IEC 14443	NFC Forum	Command Code (hexadecimal)
Anticollision	Request	REQA	SENS_REQ	26h (7 bit)
	Wake-up	WUPA	ALL_REQ	52h (7 bit)
	Anticollision CL1	Anticollision CL1	SDD_REQ CL1	93h 20h
	Select CL1	Select CL1	SEL_REQ CL1	93h 70h
	Anticollision CL2	Anticollision CL2	SDD_REQ CL2	95h 20h
	Select CL2	Select CL2	SEL_REQ CL2	95h 70h
	Halt	HLTA	SLP_REQ	50h 00h
Tag	READ	-	READ	30h
	FAST_READ	-	-	3Ah
	WRITE	-	WRITE	A2h
	COMP_WRITE	-	-	A0h
	PWD_AUTH	-	-	1Bh
	READ_SIG	-	-	3Ch
Data memory	WREN	-	-	06h
	WRDI	-	-	04h
	RDSR1	-	-	05h
	WRSR1	-	-	01h
	RDSR2	-	-	35h
	WRSR2	-	-	31h
	RDSR3	-	-	15h
	WRSR3	-	-	11h
	RDSR4	-	-	45h
	WRSR4	-	-	41h
	RDSR5	-	-	
	WRSR5			
	READ			03h
	PP	-	-	02h
	SE	-	-	20h
	BE32	-	-	52h
	BE64	-	-	D8h

Command category	Command	ISO/IEC 14443	NFC Forum	Command Code (hexadecimal)
Data memory Lock	READ_RF_DATA_RD_LOCK	-	-	65h
	READ_RF_DATA_WR_LOCK	-	-	63h
	WRITE_RF_DATA_RD_LOCK	-	-	66h
	WRITE_RF_DATA_WR_LOCK	-	-	64h
	RF_PWD_AUTH	-	-	61h

9.3.1.2 Timing

The command and response timings shown in this document are not to scale and values are rounded to 1µs.

All given command and response times refer to the data frames including start of communication and end of communication. They do not include the encoding (like the Miller pulses). A NFC device data frame contains the start of communication (1 “start bit”) and the end of communication (one logic 0 + 1 bit length of unmodulated carrier). A NFC tag data frame contains the start of communication (1 “start bit”) and the end of communication (1 bit length of no subcarrier).

The minimum command response time is specified as an integer n which specifies the NFC device to NFC tag frame delay time. The frame delay time from NFC tag to NFC device is at least 87µs. The maximum command response time is specified as a time-out value. Depending on the command, the TACK value specified for command responses defines the NFC device to NFC tag frame delay time. It does it for either the 4-bit ACK value specified in Section 9.3.1.3 or for a data frame.

All timing can be measured according to ISO/IEC 14443-3 frame specification as shown for the Frame Delay Time in Figure 94.

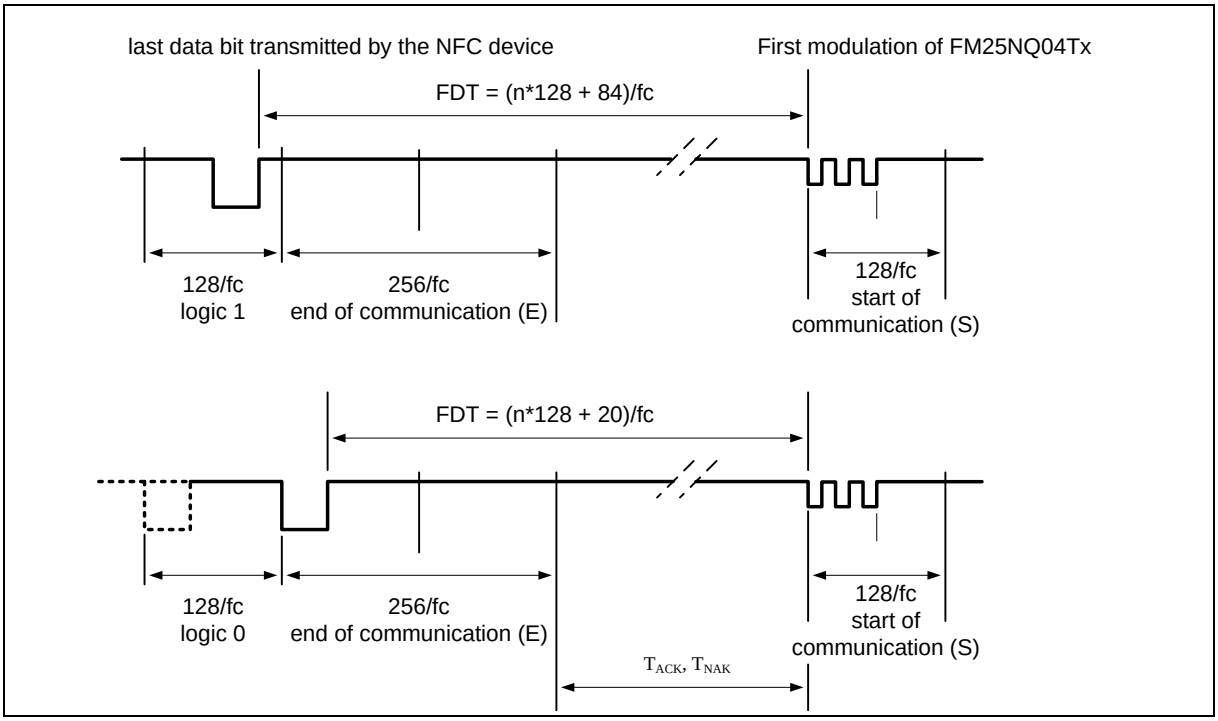


Figure 94 Frame Delay Time (from NFC device to FM25NQ04Tx), T_{ACK} and T_{NAK}

Remark: Due to the coding of commands, the measured timings usually excludes (a part of) the end of communication. Considered this factor when comparing the specified with the measured times.

9.3.1.3 ACK and NAK

When TAG memory is accessed, the device uses a 4 bit ACK / NAK as shown in Table 32.

Table 32 ACK and NAK values

Code (4-bit)	ACK/NAK
Ah	Acknowledge (ACK)
0h	NAK for invalid argument (i.e. invalid block address)
1h	NAK for parity or CRC error
5h	NAK for EEPROM write error

When DATA memory is accessed, the device uses a 1 byte ACK and 2 bytes NAK as shown in 28.

Code	ACK/NAK
0Ah	Acknowledge (ACK)
B2B2h	NAK

9.3.1.4 ATQA and SAK responses

FM25NQ04Tx replies to a REQA or WUPA command with the ATQA. It replies to a Select CL2 command with the SAK. The 2-byte ATQA value is transmitted with the least significant byte first (44h).

Table 33 ATQA response of the FM25NQ04Tx

Field	Value	Bit number															
		16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
ATQA	00 44h	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0

Table 34 SAK response of the FM25NQ04Tx

Field	Value	Bit number							
		8	7	6	5	4	3	2	1
SAK1	04h	0	0	0	0	0	1	0	0
SAK2	00h	0	0	0	0	0	0	0	0

Remark: The ATQA coding in bits 7 and 8 indicate the UID size according to ISO/IEC 14443 independent from the settings of the UID usage.

Remark: The bit numbering in the ISO/IEC 14443 starts with LSB = bit 1 and not with LSB = bit 0. So 1 byte counts bit 1 to bit 8 instead of bit 0 to 7.

9.3.2 Tag Memory command

9.3.2.1 READ(30h)

The READ command requires a start block address, and returns the 16 bytes of four blocks. For example, if address (Addr) is 03h then blocks 03h, 04h, 05h, 06h are returned. Special conditions apply if the READ command address is near the end of the accessible memory area. The special conditions also apply if at least part of the addressed blocks is within a password protected area. For details on those cases and the command structure refers to Figure 95 and Table 35. Table 36 shows the required timing.

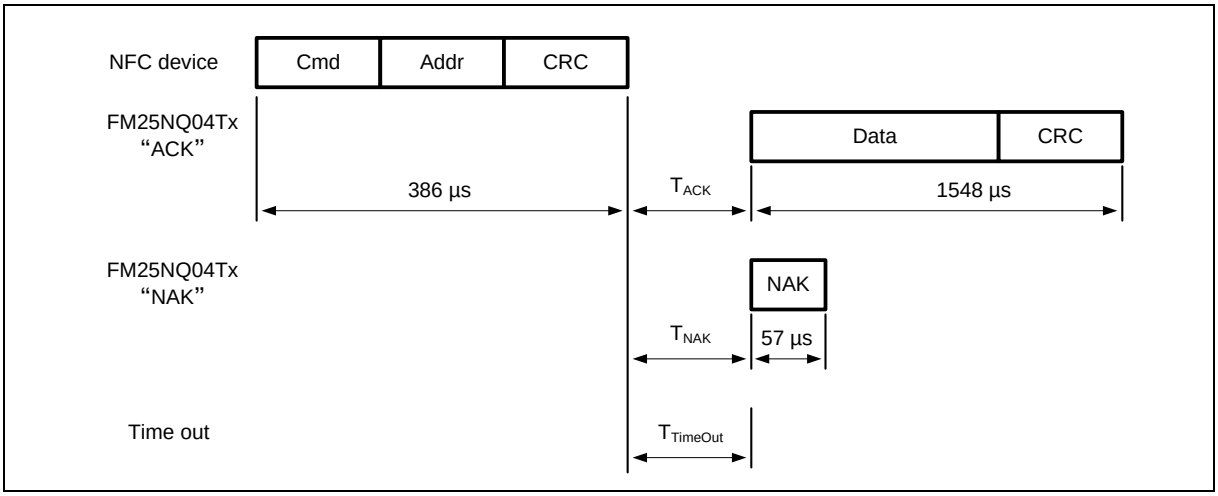


Figure 95 READ command

Table 35 READ command

Name	Code	Description	Length
Cmd	30h	read out blocks	1 byte
Addr	-	Start block address	1 byte
CRC	-	CRC	2 bytes
Data	-	Data content of the addressed blocks	16 bytes
NAK	see Table 32	see Section 9.3.1.3	4-bit

Table 36 READ timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
READ	n=9(1)	$T_{TimeOut}$	5ms

Note: 1. Refer to Section 9.3.1.2.

In the initial state of FM25NQ04Tx, all memory blocks are allowed as Addr parameter to the READ command.
- block address 00h to 2Ch for FM25NQ04T1
- block address 00h to 86h for FM25NQ04T2
- block address 00h to E6h for FM25NQ04T3

Addressing a memory block beyond the limits above results in a NAK response from FM25NQ04Tx.

A roll-over mechanism is implemented to continue reading from page 00h once the end of the accessible memory is reached. Reading from block address 2Ah on FM25NQ04Tx results in blocks 2Ah, 2Bh, 2Ch and 00h being returned.

The following conditions apply if part of the memory is password protected for read access:
- if FM25NQ04Tx is in the ACTIVE state
  - addressing a block which is equal or higher than AUTH0 results in a NAK response
  - addressing a block lower than AUTH0 results in data being returned with the roll-over mechanism occurring just before the AUTH0 defined block

• if FM25NQ04Tx is in the AUTHENTICATED state
– the READ command behaves like on a FM25NQ04Tx without access protection

Remark: PWD and PACK values can never be read out of the memory. When reading from the blocks holding those two values, all 00h bytes are replied to the NFC device instead.

9.3.2.2 FAST READ(3Ah)

The FAST_READ command requires a start block address and an end block address and returns the all n*4 bytes of the addressed blocks. For example if the start address is 03h and the end address is 07h then blocks 03h, 04h, 05h, 06h and 07h are returned. If the addressed block is outside of accessible area, FM25NQ04Tx replies a NAK. For details on those cases and the command structure, refer to Figure 96 and Table 37. Table 38 shows the required timing.

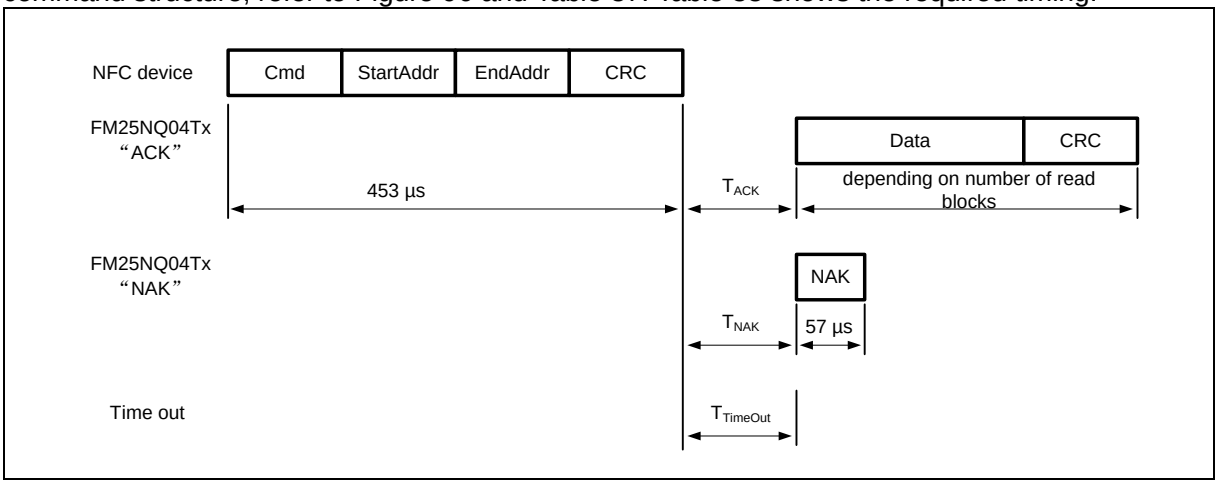


Figure 96 FAST_READ command

Table 37 FAST_READ command

Name	Code	Description	Length
Cmd	3Ah	read out multiple blocks	1 byte
StartAddr	-	start block address	1 byte
EndAddr	-	end block address	1 byte
CRC	-	CRC	2 bytes
Data	-	Data content of the addressed blocks	N*4 bytes
NAK	see Table 32	see Section 9.3.1.3	4-bit

Table 38 FAST_READ timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
FAST_READ	n=9(1)	$T_{TimeOut}$	5ms

Note: 1. Refer to Section 9.3.1.2.

In the initial state of FM25NQ04Tx, all memory blocks are allowed as StartAddr parameter to the FAST_READ command.
• block address 00h to 2Ch for FM25NQ04T1
• block address 00h to 86h for FM25NQ04T2
• block address 00h to E6h for FM25NQ04T3

Addressing a memory block beyond the limits above results in a NAK response from FM25NQ04Tx.

The EndAddr parameter must be equal to or higher than the StartAddr.

The following conditions apply if part of the memory is password protected for read access:
• if FM25NQ04Tx is in the ACTIVE state
– if any requested page address is equal or higher than AUTH0 a NAK is replied
• if FM25NQ04Tx is in the AUTHENTICATED state
– the FAST_READ command behaves like on a FM25NQ04Tx without access protection

Remark: PWD and PACK values can never be read out of the memory. When reading from the blocks holding those two values, all 00h bytes are replied to the NFC device instead.

Remark: The FAST_READ command is able to read out the whole memory with one command. Nevertheless, receive buffer of the NFC device must be able to handle the requested amount of data as there is no chaining possibility.

9.3.2.3 WRITE(A2)

The WRITE command requires a block address of tag memory, and writes 4 bytes of data into the addressed FM25NQ04Tx block. The WRITE command is shown in Figure 97 and Table 39.

Table 40 shows the required timing.

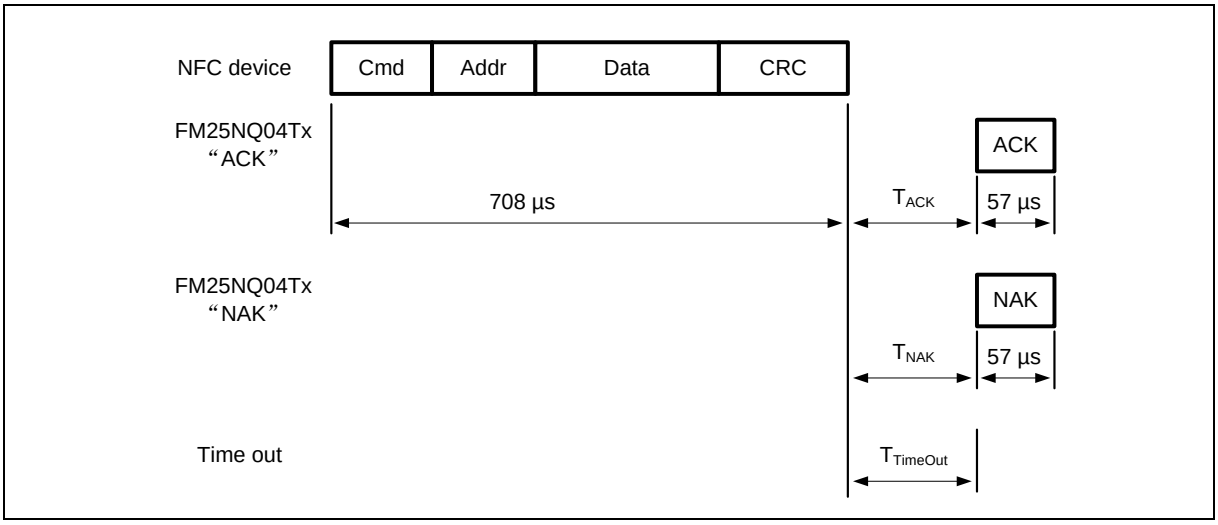


Figure 97 WRITE command

Table 39 WRITE command

Name	Code	Description	Length
Cmd	A2h	write one block	1 byte
Addr	-	block address	1 byte
CRC	-	CRC	2 bytes
Data	-	data	4 bytes
ACK	Ah	Acknowledge (ACK)	4 bit
NAK	see Table 32	see Section 9.3.1.3	4-bit

Table 40 WRITE timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
WRITE	n=9(1)	$T_{TimeOut}$	5ms

Note: 1. Refer to Section 9.3.1.2.

In the initial state of FM25NQ04Tx, the following memory blocks are valid Addr parameters to the WRITE command.
• block address 00h to 2Ch for FM25NQ04T1
• block address 00h to 86h for FM25NQ04T2
• block address 00h to E6h for FM25NQ04T3
• block address 00h of sector 0 to DFh of sector 1 for FM25NQ04T4
Addressing a memory block beyond the limits above results in a NAK response from FM25NQ04Tx. Blocks which are locked against writing cannot be reprogrammed using any write command. The locking mechanisms include static and dynamic lock bits as well as the locking of the configuration blocks.

The following conditions apply if part of the memory is password protected for write access:
• if FM25NQ04Tx is in the ACTIVE state
– writing to a blocks which address is equal or higher than AUTH0 results in a NAK response
• if FM25NQ04Tx is in the AUTHENTICATED state
– the WRITE command behaves like on a FM25NQ04Tx without access protection

FM25NQ04Tx features tearing protected write operations to specific memory content. The following blocks are protected against tearing events during a WRITE operation:
• block 2 containing static lock bits
• block 3 containing CC bits
•block 28h containing the additional dynamic lock bits for FM25NQ04T1
•block 82h containing the additional dynamic lock bits for FM25NQ04T2
•block E2h containing the additional dynamic lock bits for FM25NQ04T3
•block DBh of sector 1 containing the additional dynamic lock bits for FM25NQ04T4

9.3.2.4 COMPATIBILITY WRITE(A0h)

The COMPATIBILITY_WRITE command is implemented to guarantee interoperability with the established MIFARE Classic PCD infrastructure, in case of coexistence of ticketing and NFC applications. Even though 16 bytes are transferred to FM25NQ04Tx, only the least significant 4 bytes (bytes 0 to 3) are written to the specified address. Set all the remaining bytes, 04h to 0Fh, to logic 00h. The COMPATIBILITY_WRITE command is shown in Figure 98, Figure 99 and Table 41. Table 42 shows the required timing.

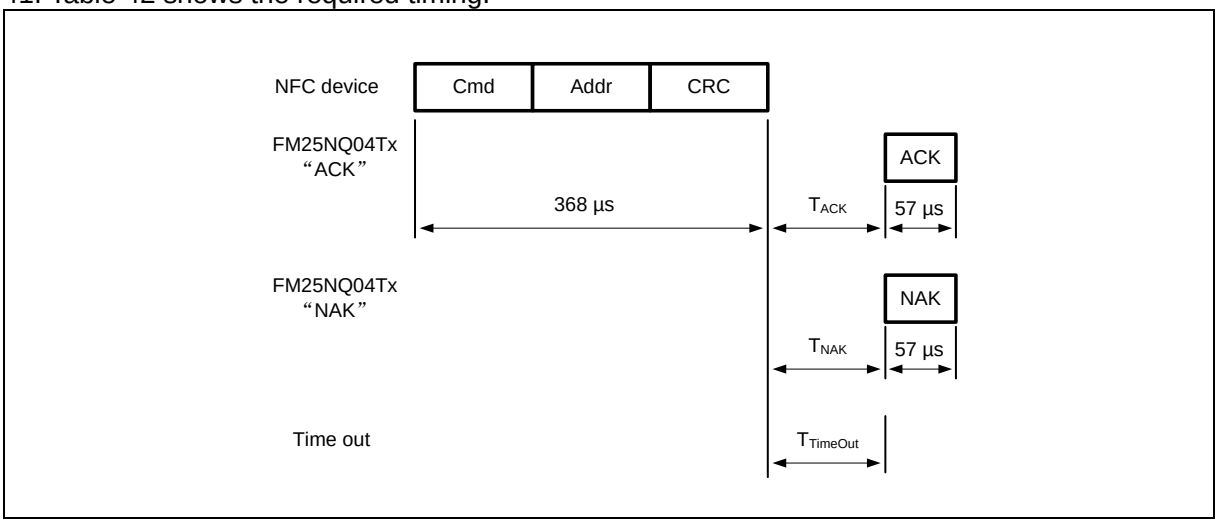


Figure 98 COMPATIBILITY_WRITE command part 1

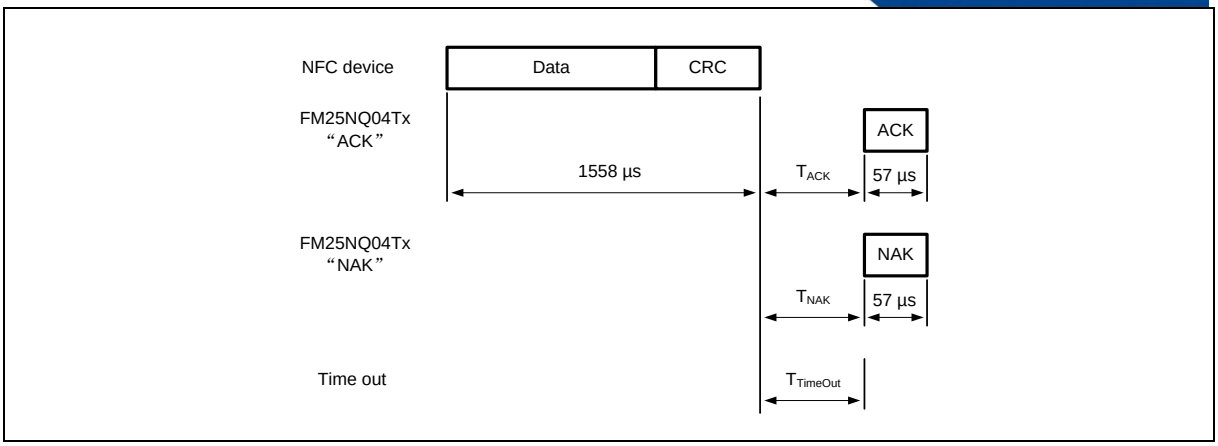


Figure 99 COMPATIBILITY_WRITE command part 2

Table 41 COMPATIBILITY_WRITE command

Name	Code	Description	Length
Cmd	A0h	Compatibility write	1 byte
Addr	-	block address	1 byte
CRC	-	CRC	2 bytes
Data	-	16-byte data, only least significant 4 bytes are written	16 bytes
ACK	Ah	Acknowledge (ACK)	4 bit
NAK	see Table 32	see Section 9.3.1.3	4-bit

Table 42 COMPATIBILITY_WRITE timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
COMPATIBILITY_WRITE part 1	n=9(1)	$T_{TimeOut}$	5ms
COMPATIBILITY_WRITE part 2	n=9(1)	$T_{TimeOut}$	10ms

Note: 1. Refer to Section 9.3.1.2.

In the initial state of FM25NQ04Tx, the following memory pages are valid Addr parameters to the COMPATIBILITY_WRITE command.

- block address 00h to 2Ch for FM25NQ04T1
- block address 00h to 86h for FM25NQ04T2
- block address 00h to E6h for FM25NQ04T3
- block address 00h of sector 0 to DFh of sector 1 for FM25NQ04T4

Addressing a memory block, that beyond the limits above, results in a NAK response from FM25NQ04Tx.

Blocks which are locked against writing cannot be reprogrammed using any write command. The locking mechanisms include static and dynamic lock bits as well as the locking of the configuration pages.

The following conditions apply if part of the memory is password protected for write access:

- If FM25NQ04Tx is in the ACTIVE state
  – Writing to a block which address is equal or higher than AUTH0 results in a NAK response
- If FM25NQ04Tx is in the AUTHENTICATED state
  – The COMPATIBILITY_WRITE command behaves the same as on a FM25NQ04Tx without access protection

FM25NQ04Tx features tearing protected write operations to specific memory content. The following pages are protected against tearing events during a COMPATIBILITY_WRITE operation:

- block 02h containing static lock bits

- block 03h containing CC bits
- block 28h containing the additional dynamic lock bits for FM25NQ04T1
- block 82h containing the additional dynamic lock bits for FM25NQ04T2
- block E2h containing the additional dynamic lock bits for FM25NQ04T3
- block DBh of sector 1 containing the additional dynamic lock bits for FM25NQ04T4

9.3.2.5 PWD AUTH(1Bh)

A protected tag memory area can be accessed only after a successful password verification using the PWD_AUTH command. The AUTH0 configuration byte defines the protected area. It specifies the first block that the password mechanism protects. The level of protection can be configured using the PROT bit either for write protection or read/write protection. The PWD_AUTH command takes the password as parameter and, if successful, returns the password authentication acknowledge, PACK. By setting the AUTHLIM configuration bits to a value larger than 000b, the number of unsuccessful password verifications can be limited. Each unsuccessful authentication is then counted in a counter featuring anti-tearing support. After reaching the limit of unsuccessful attempts, the memory access specified in PROT, is no longer possible. The PWD_AUTH command is shown in Figure 100 and Table 43. Table 44 shows the required timing.

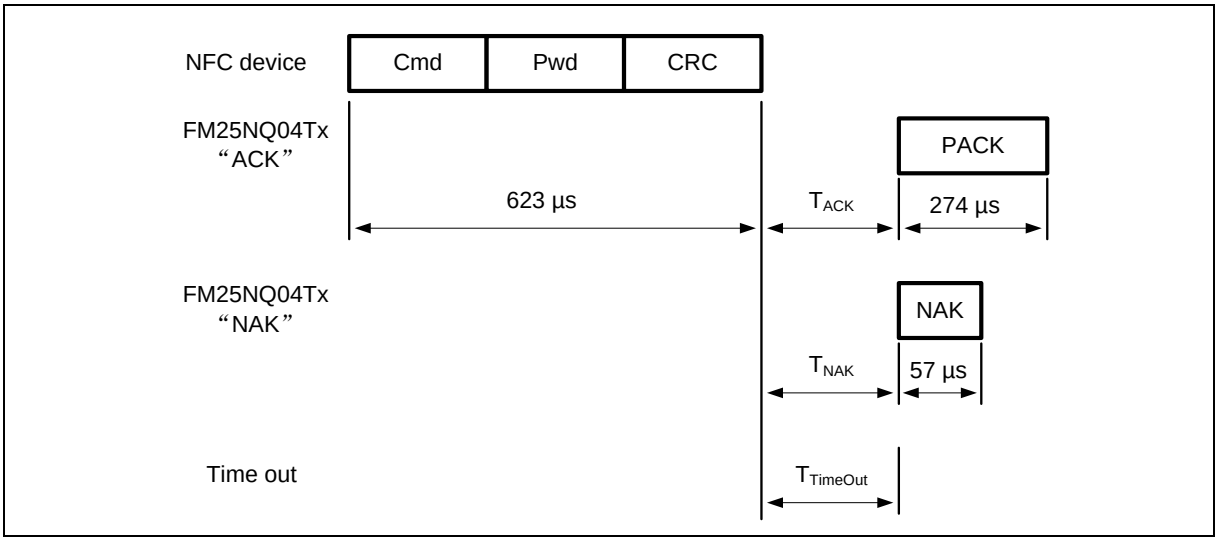


Figure 100 PWD_AUTH command

Table 43 PWD_AUTH command

Name	Code	Description	Length
Cmd	1Bh	Password authentication	1 byte
Pwd	-	password	4 byte
CRC	-	CRC	2 bytes
PACK	-	Password authentication acknowledge	2 bytes
NAK	see Table 32	see Section 9.3.1.3	4-bit

Table 44 PWD_AUTH timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
PWD_AUTH	n=9(1)	$T_{TimeOut}$	5ms

Note: 1. Refer to Section 9.3.1.2.

Remark: It is strongly recommended to change the password from its delivery state at tag issuing and set the AUTH0 value to the PWD block.

9.3.3 Data Memory Command

9.3.3.1 READ (03h)

The READ command consists of PCB, INS (03h), P1P2P3, Le byte and two CRC bytes. The first two bytes are preamble and command code that start the frame. The following three bytes P1 & P2 & P3 identify the starting address of the read operation while Le byte configures the number of data bytes to be read out. For example, if the starting address is 000100h and Le byte is 0Fh, 15 bytes data from 000100h are returned.

If the accessed memory is protected by RF_DATA_RD_LOCK in data status register 5, the response is NAK. The command structure is shown in Figure 101 and Table 45.

Table 46 shows the required timing.

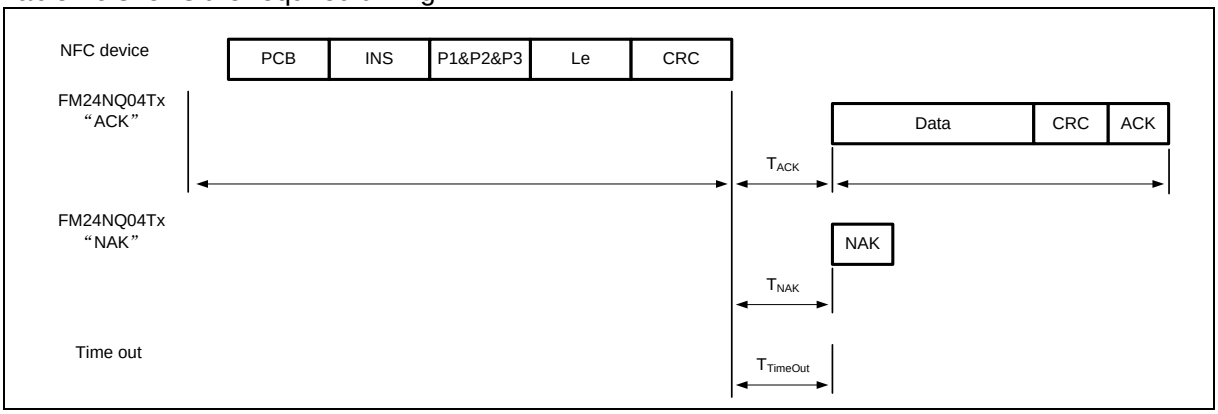


Figure 101 READ command

Table 45 READ command

Name	*Code*	*Description*	*Length*
PCB			1 byte
INS	03h	Read command	1 byte
P1 P2 P3	-	Byte address	3 bytes
Le	-	Data length(1)	1 byte
CRC	-	CRC	2 bytes
Data	-	Data output	1~256 bytes
ACK	0A		1 byte
NAK	B2B2h		2 byte

Note: 1. The number of data byte to be read is Le+1.

Table 46 READ timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
READ	n=9(1)	$T_{TimeOut}$	5ms

Note: 1. Refer to Section 9.3.1.2.

9.3.3.2 Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction

The Page Program command consists of PCB, INS (02h), P1P2P3, Lc byte, data bytes and two CRC bytes. The first two bytes are a preamble and command code that start the frame. The

following three bytes P1 & P2 & P3 identify the starting address of the Page program operation while Lc byte configures the number of data bytes to be written in. When data is transferred in, the data word address lower eight bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page.

If the data memory is protected by RF_DATA_WR_LOCK in data SR5, the response is NAK. If the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits in data SR1 and SR2, the device replies ACK but the Page Program instruction will not be executed. The command structure is shown in Figure 102 and Table 47.

Table 48 shows the required timing.

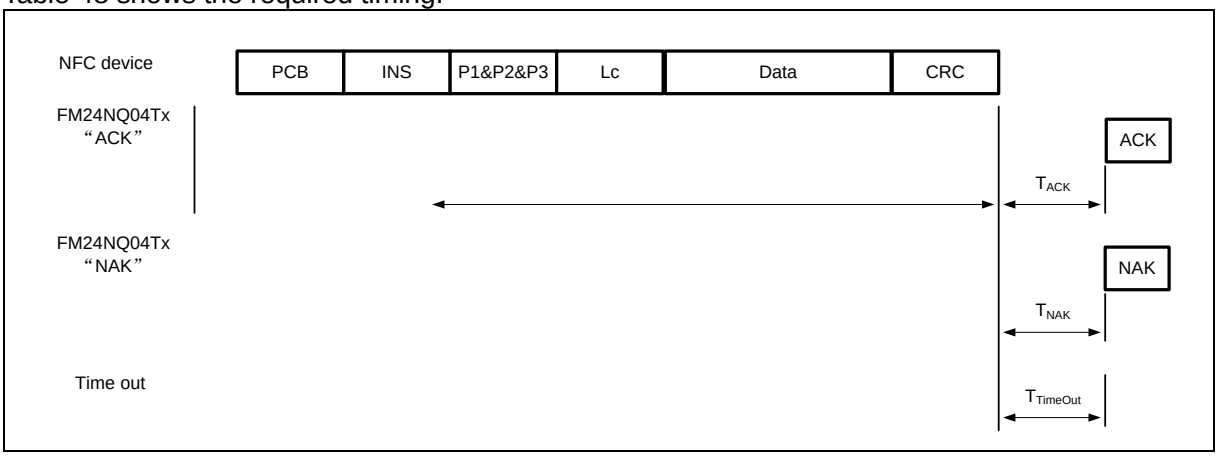


Figure 102 Page Program command

Table 47 Page Program command

Name	*Code*	*Description*	*Length*
PCB			1 byte
INS	02h	Page program command	1 byte
P1 P2 P3	-	Byte address	3 bytes
Lc	-	Data length(1)	1 byte
Data	-	Data input	1~256 bytes
CRC	-	CRC	2 bytes
ACK	A2h		1 byte
NAK	B2B2h		2 byte

Note: 1. The number of data byte to be programmed is Lc+1.

Table 48 Page Program timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
Page program	n=9(1)	$T_{TimeOut}$	5ms

Note: 1. Refer to Section 9.3.1.2.

9.3.3.3 Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1).

The Sector erase command consists of PCB, INS (20h), P1P2P3 and two CRC bytes. The first two bytes are a preamble and command code that start the frame. The following three bytes P1 & P2 & P3 identify the sector address to be erased.

If the data memory is protected by RF_DATA_WR_LOCK in data SR5, the response is NAK. If the addressed sector is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits in data SR1 and SR2, the device replies ACK but the Sector Erase instruction will not be executed. The command structure is shown in Figure 103 and Table 49.

Table 50 shows the required timing.

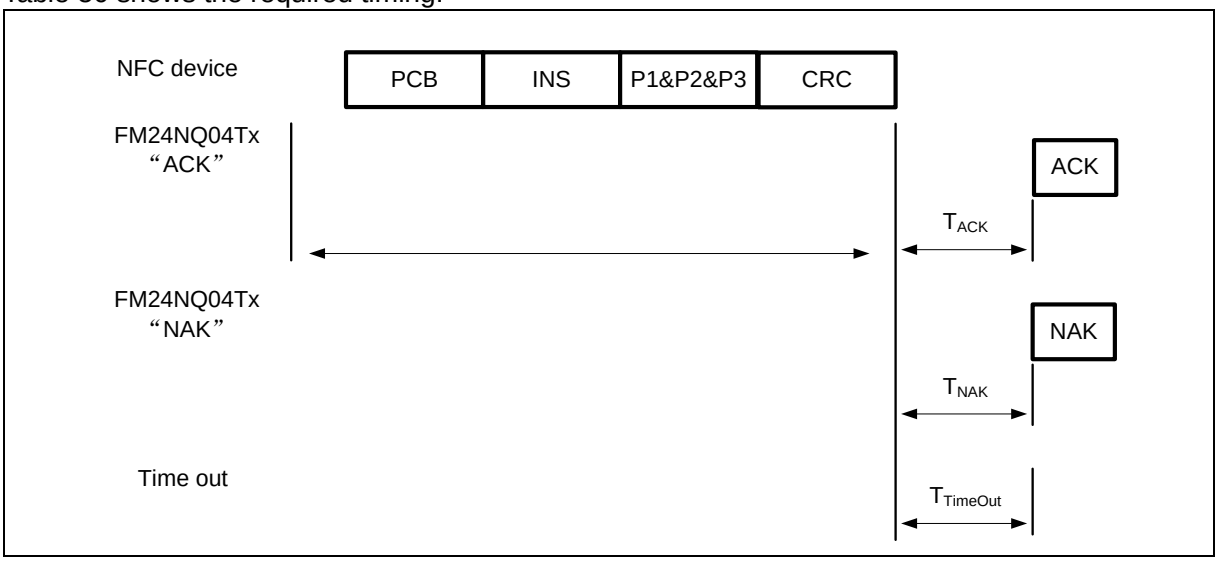


Figure 103 Sector Erase command

Table 49 Sector Erase command

Name	*Code*	*Description*	*Length*
PCB			1 byte
INS	20h	Sector erase command	1 byte
P1 P2 P3	-	Sector address	3 bytes
CRC	-	CRC	2 bytes
ACK	A2h		1 byte
NAK	B2B2h		2 byte

Table 50 Sector Erase timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
Sector erase	n=9(1)	$T_{TimeOut}$	5ms

9.3.3.4 32KB Block Erase (52h)

The 32KB Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1).

The 32KB Block erase command consists of PCB, INS (52h), P1P2P3 and two CRC bytes. The first two bytes are a preamble and command code that start the frame. The following three bytes P1 & P2 & P3 identify the block address to be erased.

If the data memory is protected by RF_DATA_WR_LOCK in data SR5, the response is NAK. If the addressed block is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits in data SR1 and SR2, the device replies ACK but the 32KB Block Erase instruction will not be executed. The command structure is shown in Figure 104 and Table 51.

Table 52 shows the required timing.

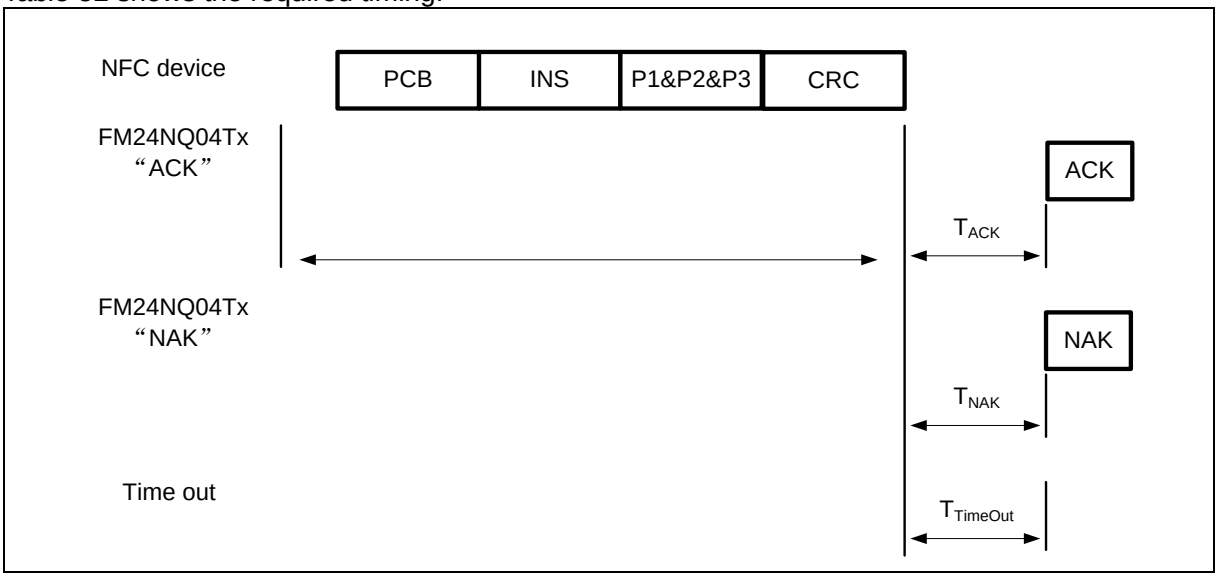


Figure 104 32KB Block Erase command

Table 51 32KB Block Erase command

Name	*Code*	*Description*	*Length*
PCB			1 byte
INS	52h	32K Block erase command	1 byte
P1 P2 P3	-	Block address	3 bytes
CRC	-	CRC	2 bytes
ACK	A2h		1 byte
NAK	B2B2h		2 byte

Table 52 32KB Block Erase timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
32K Block erase	n=9(1)	$T_{TimeOut}$	5ms

9.3.3.5 64KB Block Erase (D8h)

The 64KB Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1).

The 64KB Block erase command consists of PCB, INS (D8h), P1P2P3 and two CRC bytes. The first two bytes are a preamble and command code that start the frame. The following three bytes P1 & P2 & P3 identify the block address to be erased.

If the data memory is protected by RF_DATA_WR_LOCK in data SR5, the response is NAK. If the addressed block is protected by the Block Protect (CMP, SEC, TB, BP2, BP1, and BP0) bits in data SR1 and SR2, the device replies ACK but the 64KB Block Erase instruction will not be executed. The command structure is shown in Figure 105 and Table 53.

Table 54 shows the required timing.

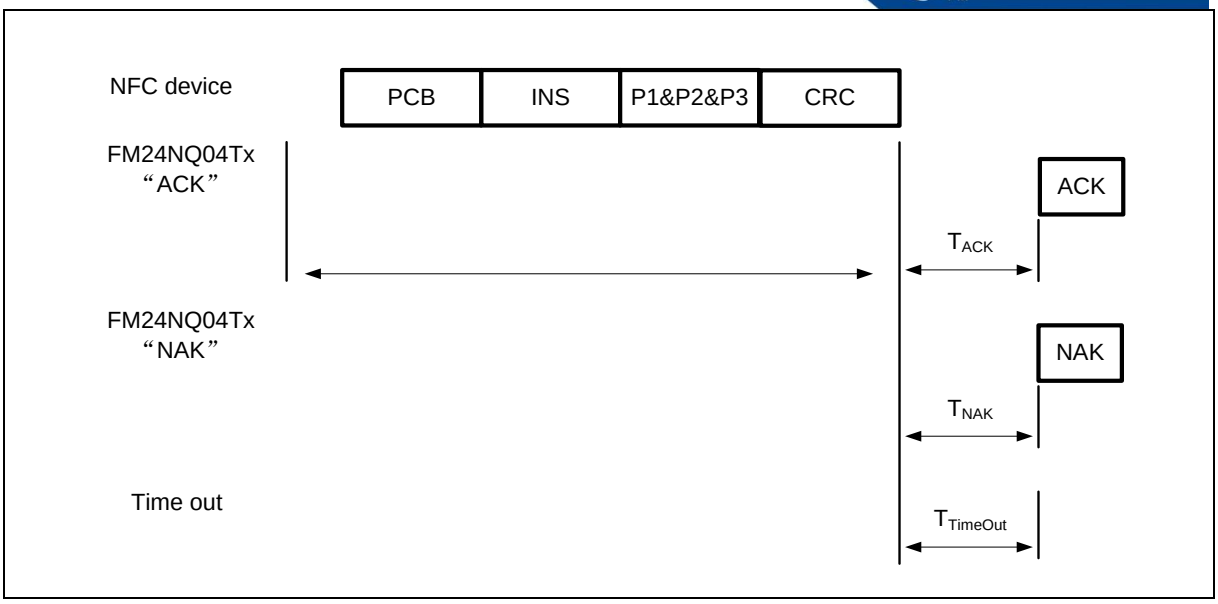


Figure 105 64KB Block Erase command

Table 53 64KB Block Erase command

Name	*Code*	*Description*	*Length*
PCB			1 byte
INS	52h	64K Block erase command	1 byte
P1 P2 P3	-	Block address	3 bytes
CRC	-	CRC	2 bytes
ACK	A2h		1 byte
NAK	B2B2h		2 byte

Table 54 64KB Block Erase timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
64K Block erase	n=9(1)	$T_{TimeOut}$	5ms

9.3.3.6 Write Enable (WREN) (06h)

The Write Enable (WREN) instruction sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase and Write Status Register instruction.

The WREN command consists of PCB, INS (06h) and two CRC bytes.

Table 56 shows the required timing.

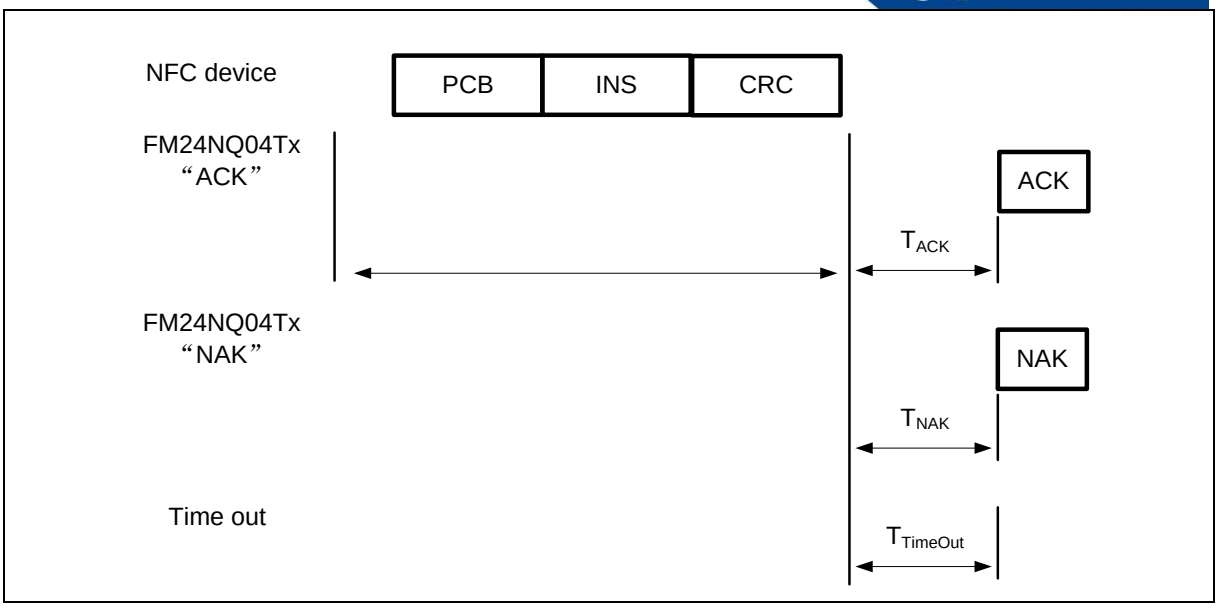


Figure 106 Write Enable command

Table 55 Write Enable command

Name	*Code*	*Description*	*Length*
PCB			1 byte
INS	06h	Write Enable command	1 byte
CRC	-	CRC	2 bytes
ACK	A2h		1 byte
NAK	B2B2h		2 byte

Table 56 Write Enable timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
Write Enable	n=9(1)	$T_{TimeOut}$	5ms

9.3.3.7 Write Disable (WRDI) (04h)

The Write Disable (WRDI) instruction resets the Write Enable Latch (WEL) bit in the Status Register to a 0. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase.

The WRDI command consists of PCB, INS (04h) and two CRC bytes.

Table 58 shows the required timing.

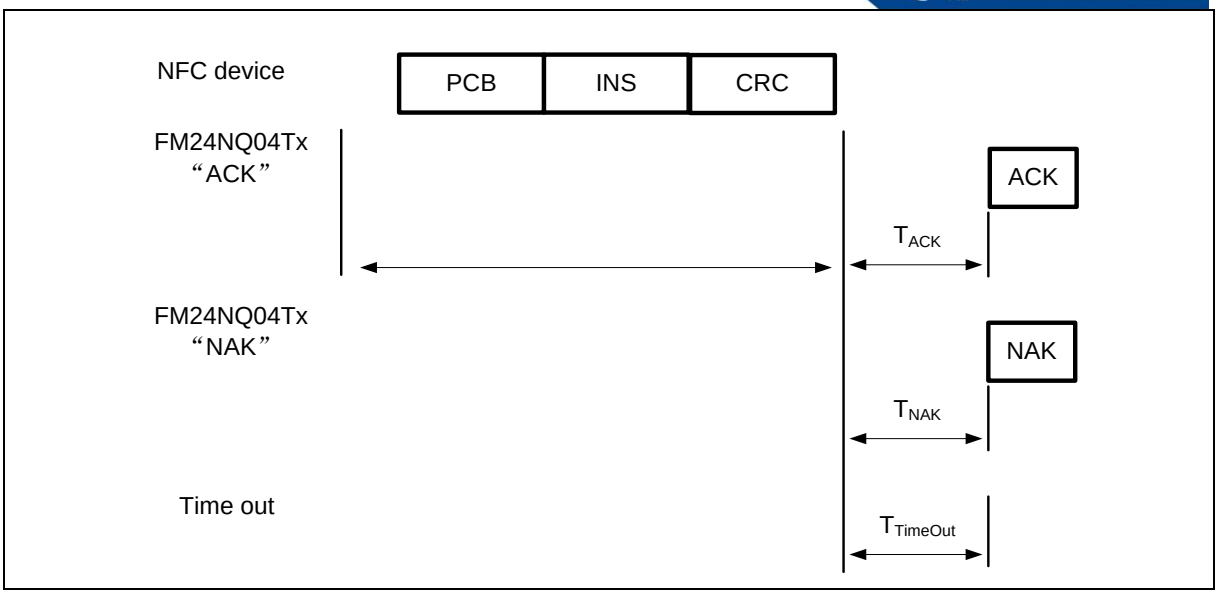


Figure 107 Write Disable command

Table 57 Write Disable command

Name	*Code*	*Description*	*Length*
PCB			1 byte
INS	04h	Write Disable command	1 byte
CRC	-	CRC	2 bytes
ACK	A2h		1 byte
NAK	B2B2h		2 byte

Table 58 Write Disable timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
Write Enable	n=9(1)	$T_{TimeOut}$	5ms

9.3.3.8 Read Status Register-1 (RDSR1) (05h) , Status Register-2 (RDSR2) (35h) & Status Register-3 (RDSR3) (15h) & Status Register-4 (RDSR5) (45h)

The Read Status Register instructions allow the 8-bit data memory Status Registers to be read.

The Read Status Register command consists of PCB, INS (05h for RDSR1, 35h for RDSR2, 15h for RDSR3 and 45h for RDSR4) and two CRC bytes.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the WIP status bit to be checked to determine when the cycle is complete and if the device can accept another instruction.

Table 60 shows the required timing.

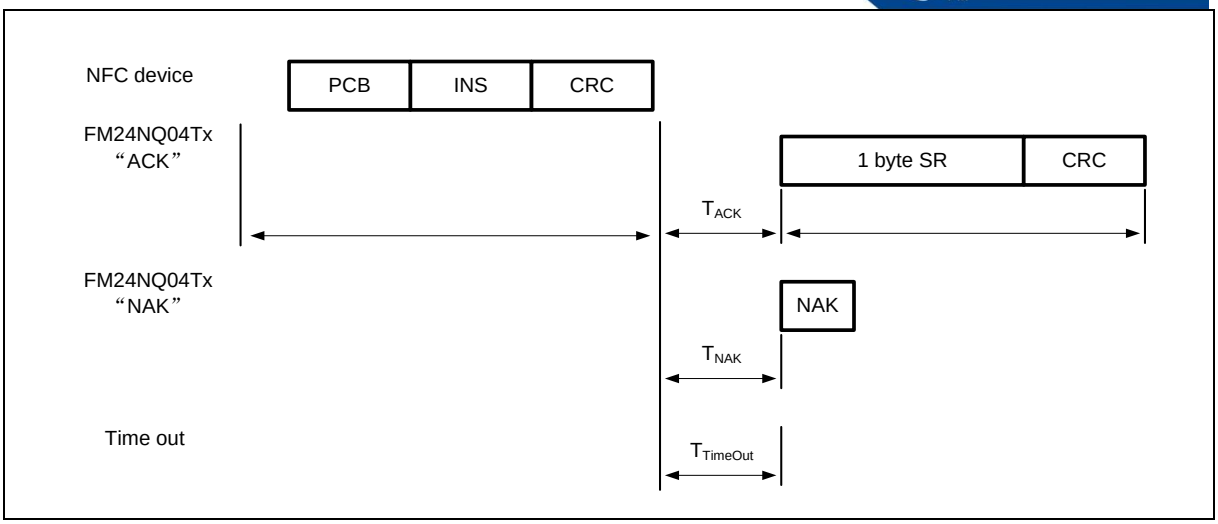


Figure 108 Write Disable command

Table 59 Read status Register command

Name	*Code*	*Description*	*Length*
PCB			1 byte
INS	05/35/15/45h	Read Status Register 1/2/3/4 command	1 byte
CRC	-	CRC	2 bytes
Data	-	Data output	1byte
ACK	A2h		1 byte
NAK	B2B2h		2 byte

Table 60 Read status Register timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
Read status Register	n=9(1)	$T_{TimeOut}$	5ms

9.3.3.9 Write Status Register-1(WRSR) (01h), Status Register-2 (31h) & Status Register-3 (11h) & Status Register-4 (41h)

The Write Status Register (WRSR) instruction allows the data memory Status Register to be written. Only non-volatile Status Register bits SRP0, SEC, TB, BP2, BP1, BP0 (bits 7 thru 2 of Status Register-1) , CMP, LB1, LB0 QE, SRP1 (bits 12 thru 8 of Status Register-2) , WPS, DRV0, DRV1(bits 2 thru 0 of Status Register-3) and PTB, PD6-PD0(Status Register-4) can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register (WRSR) instruction. LB1-0 are non-volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

To write Status Register, a Write Enable (06h) instruction must previously have been executed for the device to accept the Write Status Register (WRSR) instruction (Status Register bit WEL must equal 1).

The Write Status Register command consists of PCB, INS (01h for WRSR1, 31h for WRSR2, 11h for WRSR3 and 41h for WRSR4), one data byte and two CRC bytes.

Table 62 shows the required timing.

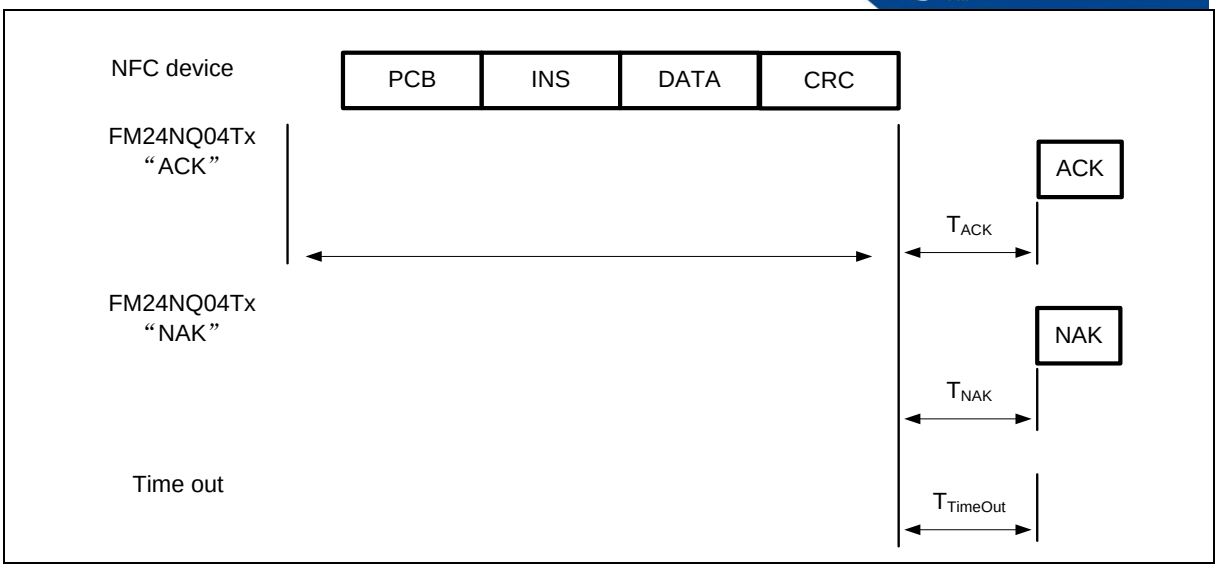


Figure 109 Write Disable command

Table 61 Write status Register command

Name	*Code*	*Description*	*Length*
PCB			1 byte
INS	01/31/11/41h	Write Status Register 1/2/3/4 command	1 byte
DATA	-	Data byte	1 byte
CRC	-	CRC	2 bytes
Data	-	Data output	1byte
ACK	A2h		1 byte
NAK	B2B2h		2 byte

Table 62 Write status Register timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
Write status Register	n=9(1)	$T_{TimeOut}$	5ms

9.3.4 Data Memory Lock Command

9.3.4.1 READ_RF_DATA_RD_LOCK (6Ah)

The READ_RF_DATA_RD_LOCK command is used to read the byte of RF_DATA_RD_ LOCK which is the first byte of data status register 5. 32 bytes of data would be transferred but only the first byte makes sense, all the following 31 bytes are 00h. The command structure is shown in Figure 110 and Table 63. Table 64 shows the required timing.

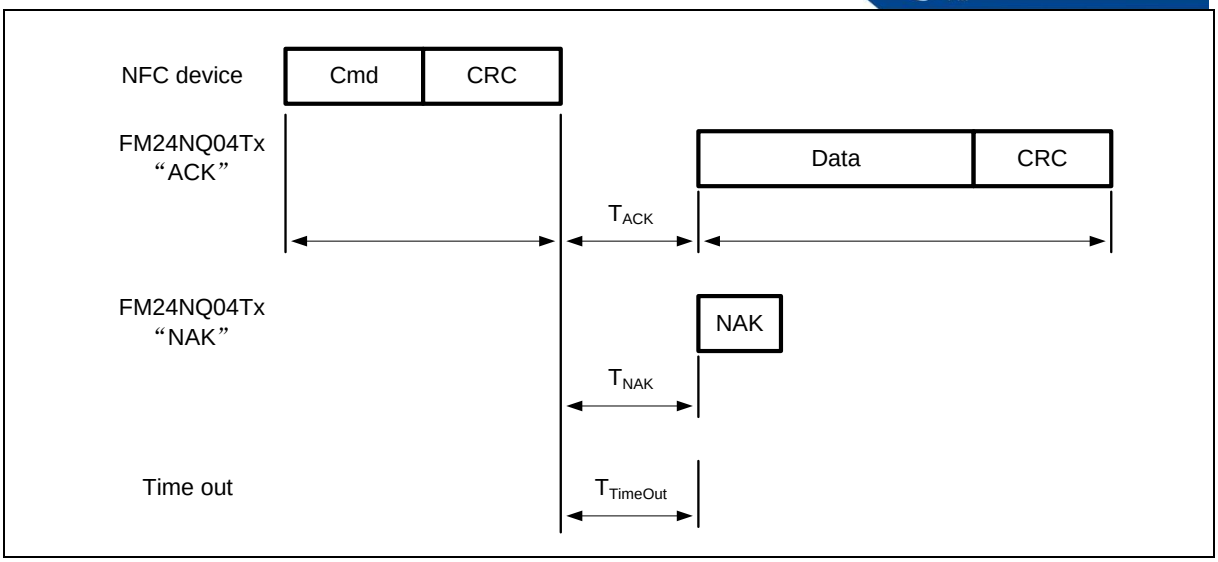


Figure 110 READ_RF_DATA_RD_LOCK command

Table 63 READ_RF_DATA_RD_LOCK command

Name	Code	Description	Length
Cmd	6Ah	Read RF_DATA_RD_LOCK data	1 byte
CRC	-	CRC	2 bytes
Data	-	data	32 bytes, only first byte makes sense
NAK	see Table 32	see Section 9.3.1.3	4 bit

Table 64 READ_RF_DATA_RD_LOCK timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
READ_RF_DATA_RD_LOCK	n=9(1)	$T_{TimeOut}$	5ms

Note: 1. Refer to Section 9.3.1.2.

9.3.4.2 READ_RF_DATA_WR_LOCK (6Ch)

The READ_RF_DATA_WR_LOCK command is used to read byte of RF_DATA_WR_LOCK which is the second byte of data status register 5. 32 bytes of data would be transferred but only the first byte makes sense, all the following 31 bytes are 00h. The command structure is shown in Figure 111 and Table 65.

Table 66 shows the required timing.

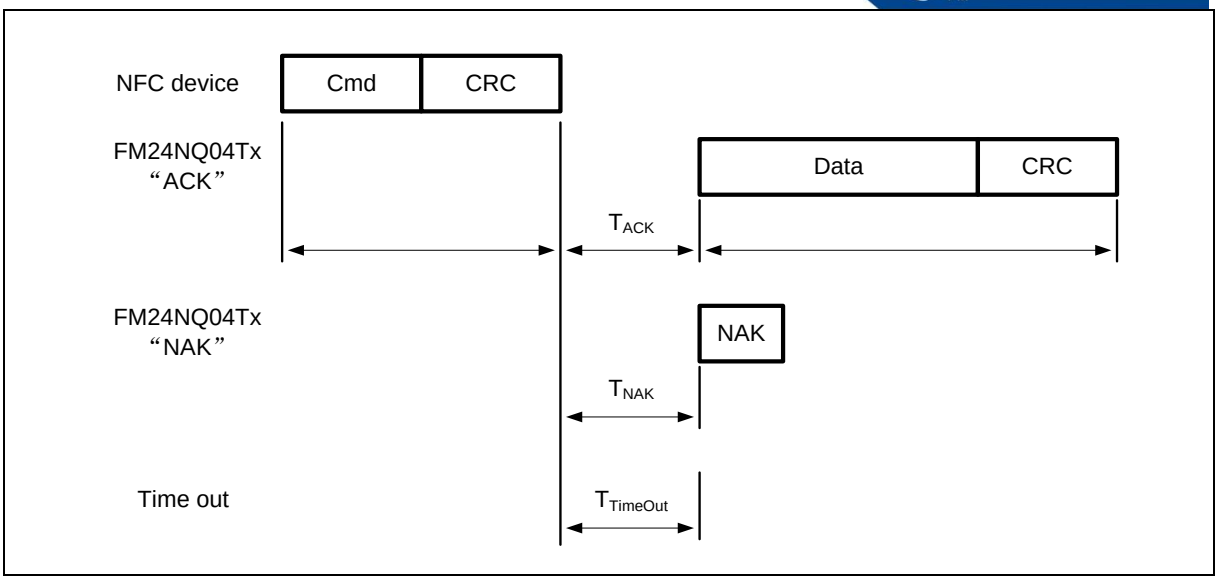


Figure 111 READ_RF_DATA_WR_LOCK command

Table 65 READ_RF_DATA_WR_LOCK command

Name	Code	Description	Length
Cmd	6Ch	Read RF_DATA_WR_LOCK data	1 byte
CRC	-	CRC	2 bytes
Data	-	data	32 bytes, only the first byte makes sense
NAK	see Table 32	see Section 9.3.1.3	4 bit

Table 66 READ_RF_DATA_WR_LOCK timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
READ_RF_DATA_WR_LOCK	n=9(1)	$T_{TimeOut}$	5ms

Note: 1. Refer to Section 9.3.1.2.

9.3.4.3 WRITE_RF_DATA_RD_LOCK (7Fh)

The WRITE_RF_DATA_RD_LOCK command writes 32 bytes of data into the RF_DATA_RD_LOCK in data status register 5. Only the first byte makes sense, the following 31 bytes can be any value. This command is executed in DM AUTHENTICATED state. If the RF_DATA_PWD is not authenticated, the response of this command is NAK. The WRITE_RF_DATA_RD_LOCK command is bit-wise OR'ed. It can change lock bit to logic 1, but cannot change back to logic 0.The WRITE_RF_DATA_RD_LOCK command is shown in Figure 112 and Table 67.

Table 68 shows the required timing.

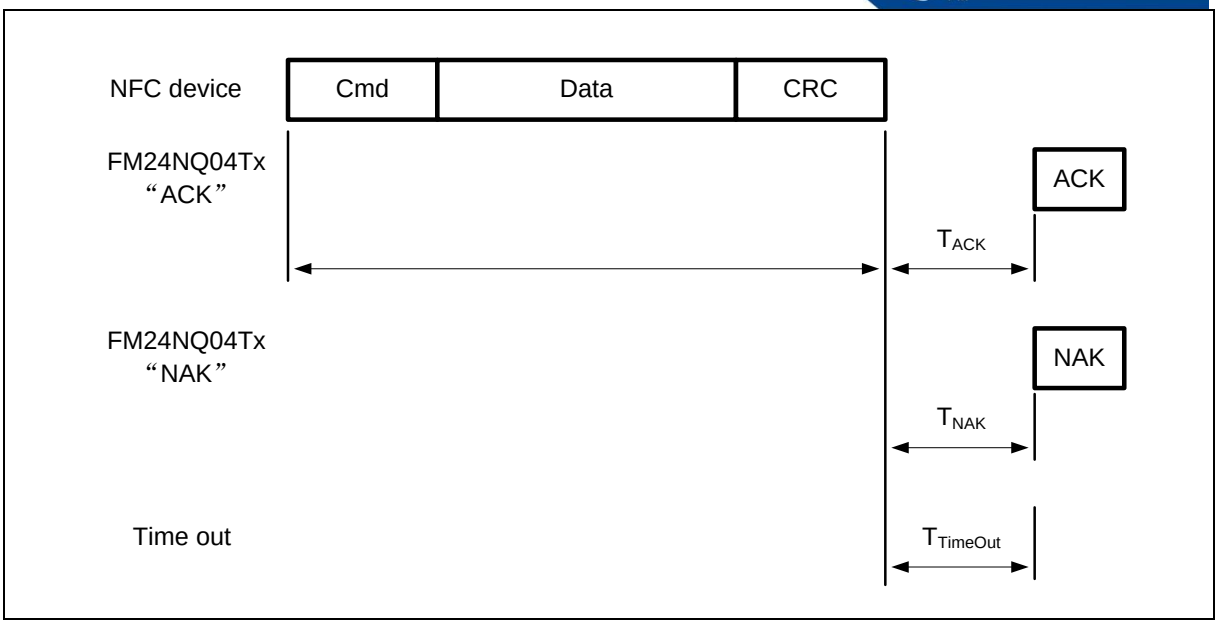


Figure 112 WRITE_RF_DATA_RD_LOCK command

Table 67 WRITE_RF_DATA_RD_LOCK command

Name	Code	Description	Length
Cmd	7Fh	write RF_DATA_RD_LOCK data	1 byte
Data	-	data	32 bytes, only the first byte makes sense
CRC	-	CRC	2 bytes
ACK	Ah	Acknowledge (ACK)	4 bit
NAK	see Table 32	see Section 9.3.1.3	4 bit

Table 68 WRITE_RF_DATA_RD_LOCK timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
WRITE_RF_DATA_RD_LOCK	n=9(1)	$T_{TimeOut}$	5ms

Note: 1. Refer to Section 9.3.1.2.

9.3.4.4 WRITE_RF_DATA_WR_LOCK (7Eh)

The WRITE_RF_DATA_WR_LOCK command writes 32 bytes of data into the RF_DATA_WR_LOCK in data status register 5. Only the first byte makes sense, the following 31 bytes can be any value. This command is executed in DM AUTHENTICATED state. If the RF_DATA_PWD is not authenticated, the response of this command is NAK. This command is bit-wise OR’ed. It can change lock bit to logic 1, but cannot change back to logic 0. The WRITE_RF_DATA_WR_LOCK command is shown in Figure 113 and Table 69.

Table 70 shows the required timing.

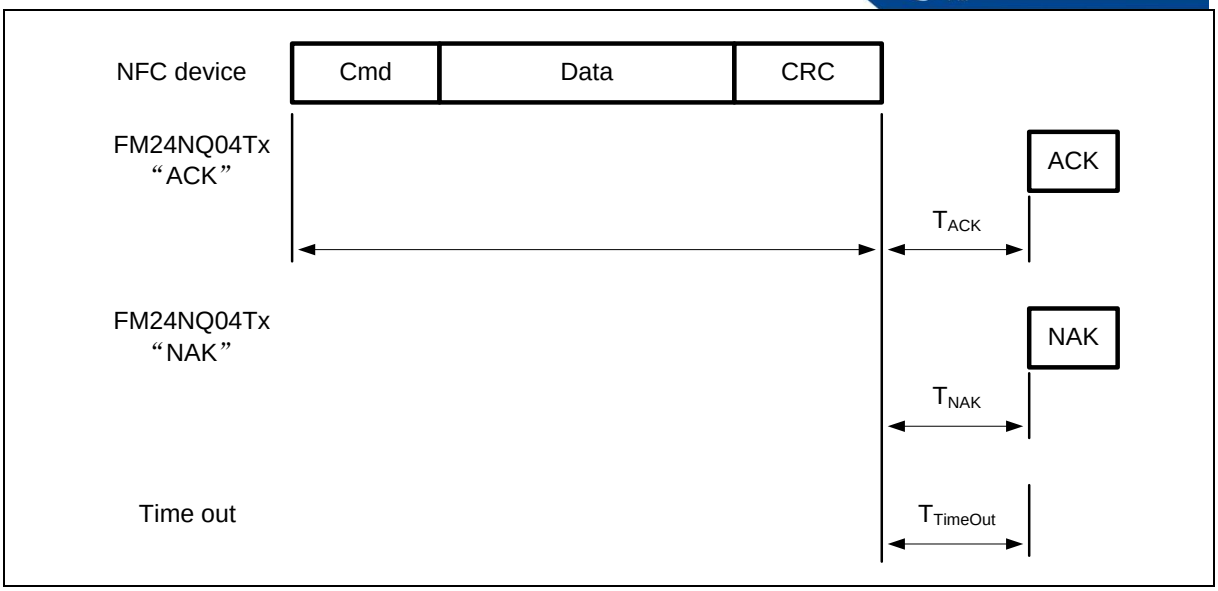


Figure 113 WRITE_RF_DATA_WR_LOCK command

Table 69 WRITE_RF_DATA_WR_LOCK command

Name	Code	Description	Length
Cmd	7Eh	write RF_DATA_WR_LOCK data	1 byte
Data	-	data	32 bytes, only the first byte makes sense
CRC	-	CRC	2 bytes
ACK	Ah	Acknowledge (ACK)	4 bit
NAK	see Table 32	see Section 9.3.1.3	4 bit

Table 70 WRITE_RF_DATA_WR_LOCK timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
WRITE_RF_DATA_WR_LOCK	n=9(1)	$T_{TimeOut}$	5ms

Note: 1. Refer to Section 9.3.1.2.

9.3.4.5 RF_PWD_AUTH (40h)

RF_DATA_RD_LOCK & RF_DATA_WR_LOCK in data status register 5 can be changed only after a successful password verification using the RF_PWD_AUTH command. The RF_PWD_AUTH command takes the password as parameter and, if successful, returns ACK. The RF_PWD_AUTH command is shown in Figure 114 and Table 71.

Table 72 shows the required timing.

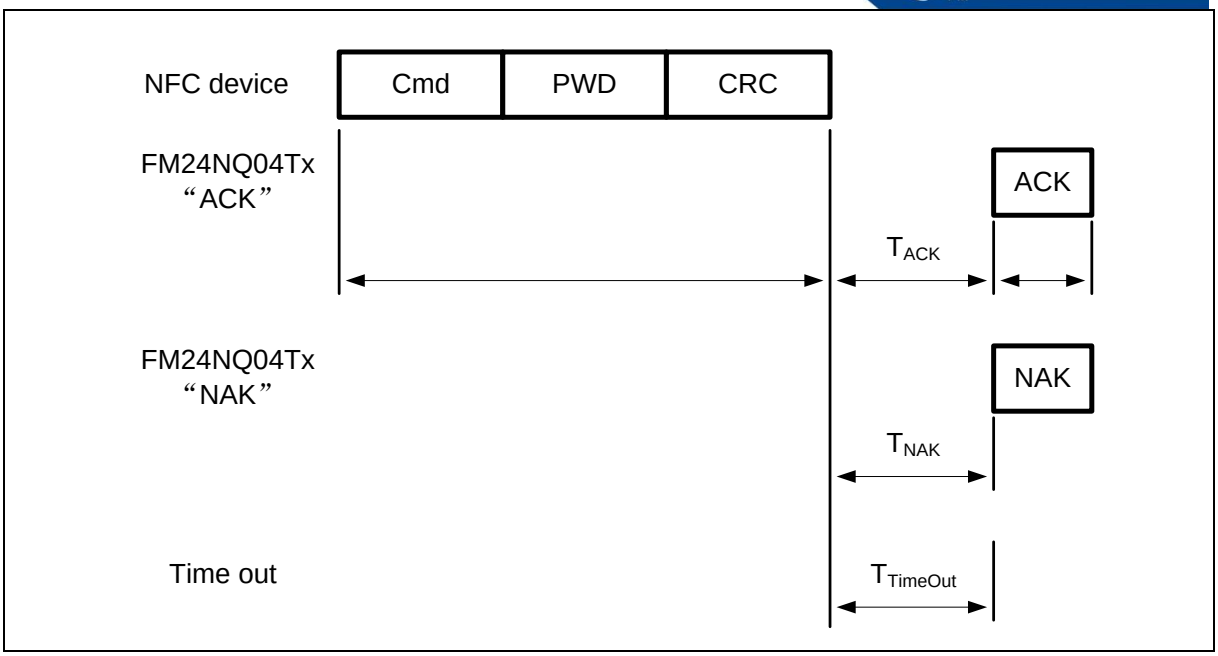


Figure 114 RF_PWD_AUTH command

Table 71 RF_PWD_AUTH command

Name	Code	Description	Length
Cmd	40h	RF password authentication	1 byte
PWD	-	RF_PWD	4 bytes
CRC	-	CRC	2 bytes
ACK	-	ACK	4 bit
NAK	see Table 32	see Section 9.3.1.3	4 bit

Table 72 RF_PWD_AUTH timing

These times exclude the end of communication of the NFC device.

Cmd	$T_{ACK/NAK}$ min	$T_{ACK/NAK}$ max	$T_{TimeOut}$
RF_PWD_AUTH	n=9(1)	$T_{TimeOut}$	5ms

Note: 1. Refer to Section 9.3.1.2.

10 Dual-interface Arbitrating

FM25NQ04Tx can be accessed by SPI (contact) interface or RF interface. There are four parts of memory in the device, which are data memory including data status register 1~4, data status register 5, tag memory and tag status registers. In some condition, simultaneous access from two interfaces is allowed.

- Data memory and one of the rest three parts can be accessed by two interfaces respectively at same time.
- Data status register 5 and one of tag memory or tag status registers can be accessed by two interfaces respectively at same time except for both write operation.

In other conditions, collision happens when two interfaces access the device at same time, and a 'First come, first serve' strategy is performed.

EH_FD and GPO pin help the master of SPI interface understand RF interface operation in order to select the right time to send command.

11 Electrical Characteristics

11.1 Absolute Maximum Ratings

Table 73 Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
Top	Operating temperature	-55	125	°C
T_{STG}	Storage temperature	-65	150	°C
V_{IO}	Contact input or output range	-0.5	V_{CC}+0.4	V
V_{CC}	Contact supply voltage	-0.5	4.0	V
V_{IN_1}	RF input voltage amplitude peak to peak between IN1 and IN2, VSS pin left floating		15	V
V_{IN_2}	AC voltage between IN1 and VSS, or IN2 and VSS	-1	15	V
I_{IN}	RF supply current IN1 – IN2		40	mA
V_{OP}	Maximum operating voltage		4.0	V
Io	DC output current on pin GPO		5.0	mA

Remark: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

11.2 Contact interface

11.2.1 Pin Capacitance

Table 74 Input capacitance of contact pin

Symbol	Parameter	Condition	Min	Max	Unit
C_{IN}(1)	Input capacitance (input pin)	V_{IN} = 0V, f = 1MHz		6	pF
	Input capacitance (I/O pin)	$V_{I/O}$ = 0V, f = 1MHz		8	pF

Note: 1. This parameter is characterized and is not 100% tested.

11.2.2 DC Characteristics

Table 75 Operating conditions of contact interface

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	2.7	3.6	V
T_A	Ambient operating temperature	-40	85	℃

Table 76 DC characteristics of contact interface

Applicable over recommended operating range from: T_A = -40°C to +85°C, V_{CC} = +1.7V to +5.5V, (unless otherwise noted).

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{CC1}	Standby Current	V_{CC}=3.6V, CS# = V_{CC}, V_{IN} = Vss or V_{CC}		1	5	μA
I_{CC2}	Deep Power-down	V_{CC}=3.6V, CS# = V_{CC},		1	5	μA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	Current	V_{IN} = Vss or V_{CC}				
I_{CC3}	Read Data Current (1)	V_{CC}=3.6V,CLK=0.1, V_{CC}/0.9V_{CC} at 10MHz, DQ open			15	mA
I_{CC4}	Operating Current (WRSR)	V_{CC}=3.6V,CS#=V_{CC}		8	12	mA
I_{CC5}	Operating Current (PP)	V_{CC}=3.6V,CS#=V_{CC}		20	25	mA
I_{CC6}	Operating Current (SE)	V_{CC}=3.6V,CS#=V_{CC}		20	25	mA
I_{CC7}	Operating Current (BE)	V_{CC}=3.6V,CS#=V_{CC}		20	25	mA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC}/V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC}/V_{SS}		0.05	3.0	µA
V_{IL} (1)	Input Low Level		-0.6		V_{CC} x 0.3	V
V_{IH} (1)	Input High Level		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level 2	V_{CC} = 3.0V, I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level 1	V_{CC} =1.7V, I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

11.2.3 AC Characteristics

Table 77 AC measurement conditions of contact interface

Symbol	Parameter	Min	Max	Unit
C_L	Load capacitance		20	pF
R_L	Load resistor connected to V_{CC}	1.3		kΩ
t_R, t_F	Input rise and fall times		5	ns
V_{IN}	Input levels	0.2V_{CC} to 0.8V_{CC}		V
$V_{REF(t)}$	Input and output timing reference levels	0.5V_{CC}		V

Table 78 AC characteristics of contact interface

Applicable over recommended operating range from: T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V, (unless otherwise noted).

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
F_{R1}	Serial Clock Frequency for: Data memory and data memory status register 1~4 operation			10	MHz
F_{R2}	Serial Clock Frequency for: Tag memory, tag memory status register and data memory status register 5 operation			2.5	MHz
t_{CH1} (1)	Serial Clock High Time for F_{R1}	45			ns
t_{CL1} (1)	Serial Clock Low Time for F_{R1}	60			ns
t_{CH2} (1)	Serial Clock High Time for F_{R2}	180			ns
t_{CL2} (1)	Serial Clock Low Time for F_{R2}	240			ns

SYMBOL	PARAMETER	SPEC			UNIT
		MIN	TYP	MAX	
t_{CLCH}(2)	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CHCL}(2)	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
t_{SLCH}	CS# Active Setup Time	70			ns
t_{CHSH}	CS# Active Hold Time	50			ns
t_{SHCH}	CS# Not Active Setup Time	50			ns
t_{CHSL}	CS# Not Active Hold Time	50			ns
t_{SHSL1}	CS# High Time (for Array Read → Array Read)	70			ns
t_{SHSL2}	CS# High Time (for Erase or Program → Read Status Registers) Volatile Status Register Write Time	100			ns
t_{SHQZ}(2)	Output Disable Time			10	ns
t_{CLQX}	Output Hold Time95	0			ns
t_{DVCH}	Data In Setup Time	5			ns
t_{CHDX}	Data In Hold Time	10			ns
t_{HLCH}	HOLD# Low Setup Time (relative to CLK)	10			ns
t_{HHCH}	HOLD# High Setup Time (relative to CLK)	10			ns
t_{CHHH}	HOLD# Low Hold Time (relative to CLK)	10			ns
t_{CHHL}	HOLD# High Hold Time (relative to CLK)	10			ns
t_{HLQZ}(2)	HOLD# Low to High-Z Output			25	ns
t_{HHQX}(2)	HOLD# High to Low-Z Output			15	ns
t_{CLQV}	Output Valid from CLK			60	ns
t_{WHSL}	Write Protect Setup Time before CS# Low	50			ns
t_{SHWL}	Write Protect Hold Time after CS# High	200			ns
t_{DP}(2)	CS# High to Deep Power-down Mode			3	μs
t_{RES1}(2)	CS# High to Standby Mode without Electronic Signature Read			3	μs
t_{RES2}(2)	CS# High to Standby Mode with Electronic Signature Read			1.8	μs
t_{SUS}(2)	CS# High to next Instruction after Suspend			20	μs
t_{RST}(2)	CS# High to next Instruction after Reset			20	μs
t_W	Write Status Register Cycle Time		10	15	ms
t_{PP}	Page Programming Time		1.5	5	ms
t_{SE}	Sector Erase Time		0.09	0.3	s
t_{BE}	Block Erase Time (32KB)		0.3	1.8	s
t_{BE}	Block Erase Time (64KB)		0.5	2	s
t_{CE}	Chip Erase Time		32	128	s

Notes:

1. $T_{CH1}+T_{CL1} >= 1 / F_{R1}$, $T_{CH2}+T_{CL2} >= 1 / F_{R2}$
2. This parameter is characterized and is not 100% tested.

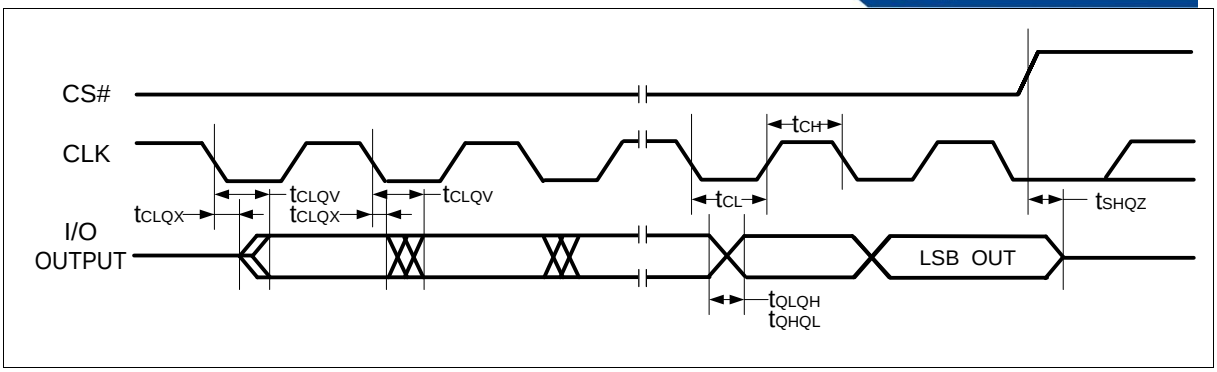


Figure 115 Serial Output Timing

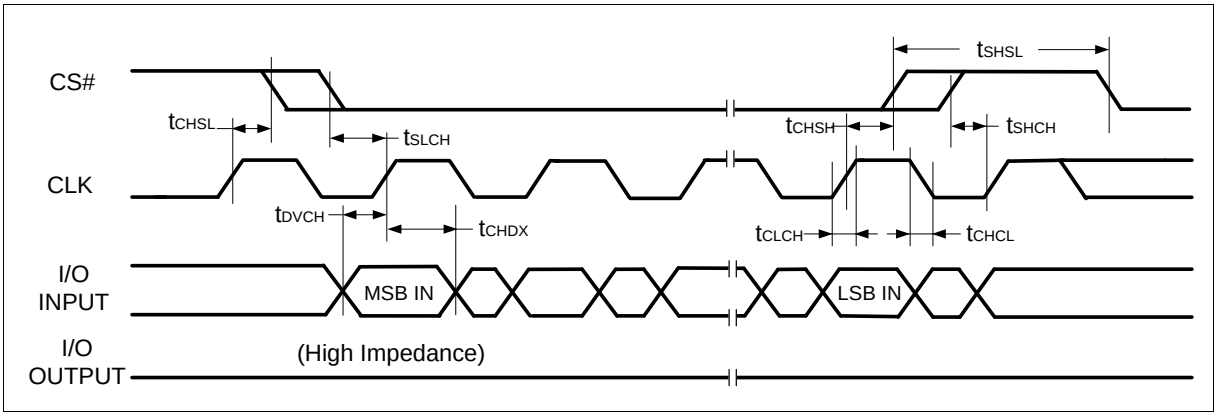


Figure 116 Serial Input Timing

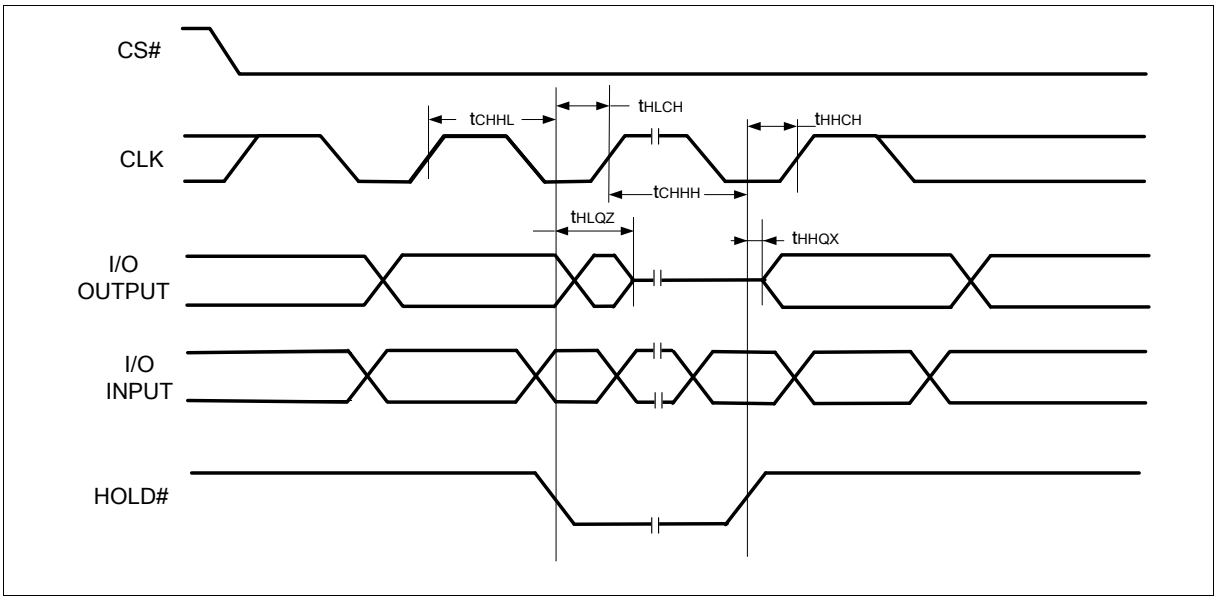


Figure 117 Hold Timing

Note: 1. This parameter is characterized and is not 100% tested.

2. SPI interface timeout.

11.2.4 Power-up Timing

Applicable over recommended operating range from: T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V, (unless otherwise noted).

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to CS# Low	t_{VSL}	10		µs
Time Delay Before Write Instruction	t_{PUW}	1	10	ms
Write Inhibit Threshold Voltage	V_{WI}	1	2	V

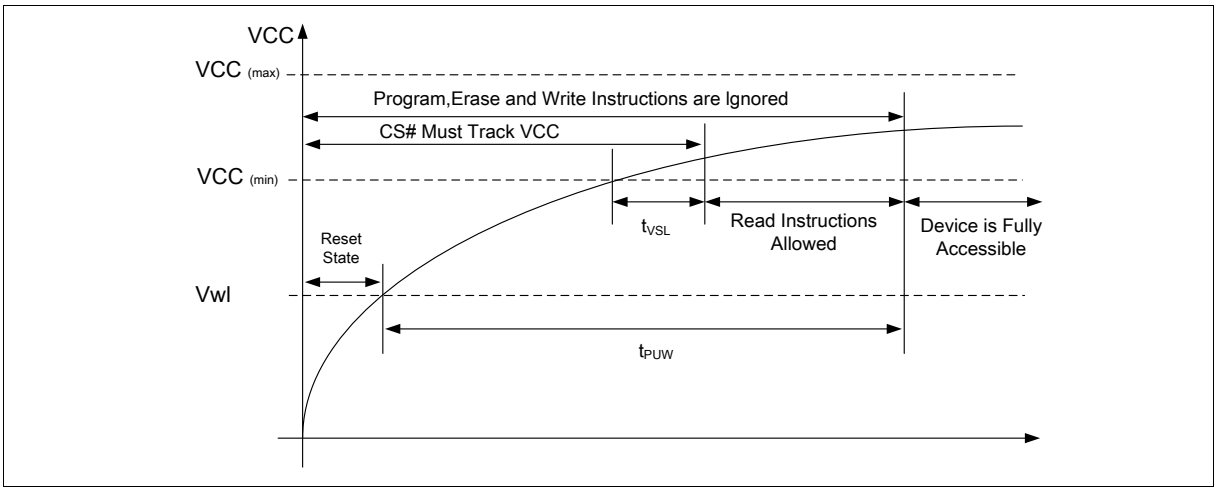


Figure 118 Power-up Timing

11.3 RF interface

Table 79 characteristics of RF interface

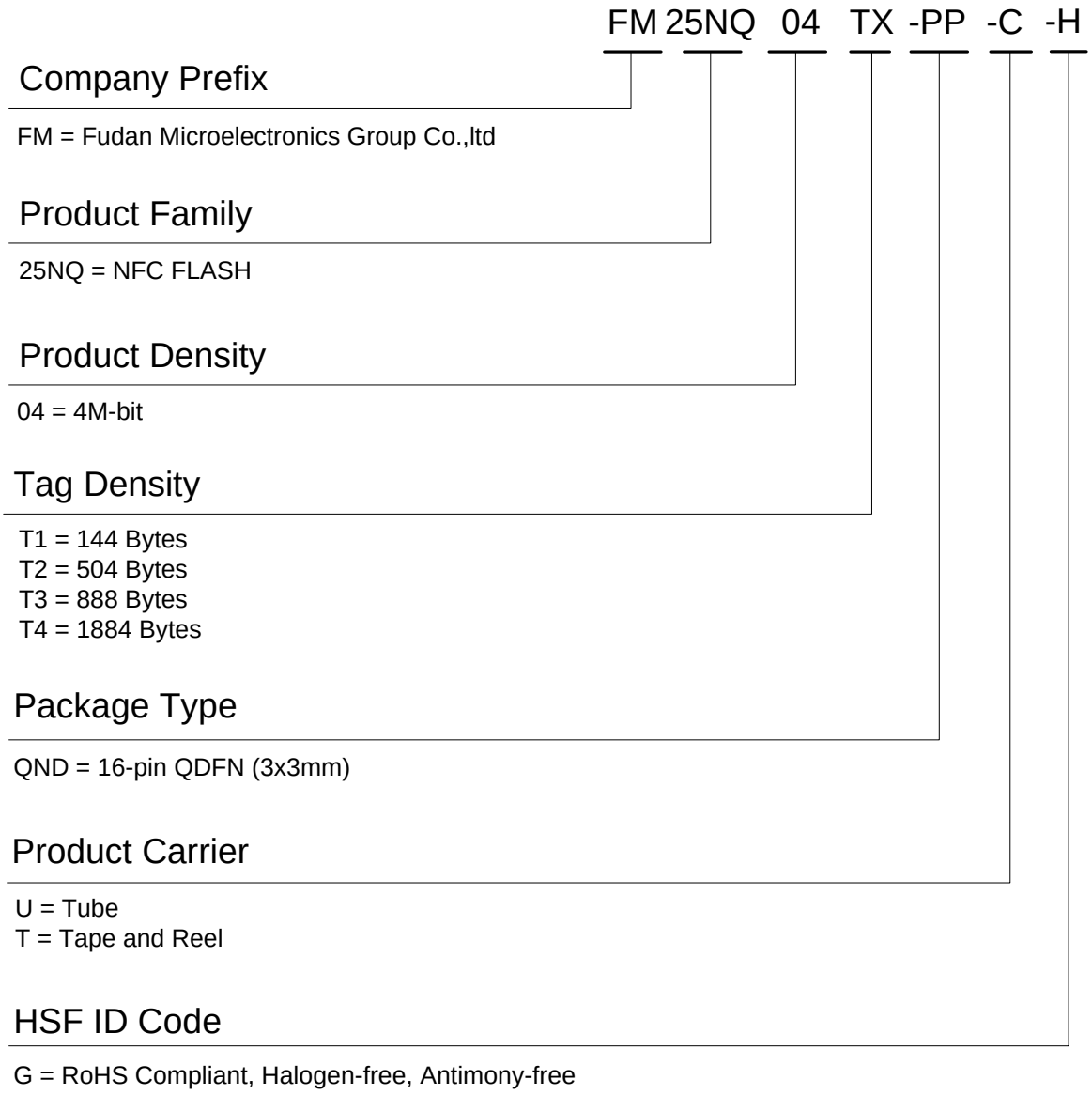
Applicable over recommended operating range from: T_A = -40°C to +85°C, V_{CC} = +2.7V to +3.6V, (unless otherwise noted).

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_C	RF carrier frequency		13.553	13.560	13.567	MHz
H_ISO	Operating field according to ISO	T_A= -40℃ to 85℃	1.5		7.5	A/m
Ci	Input capacitance(IN1 to IN2)	(1)			6	pF
V_{FD1}	Field detect output voltage	EH_FD_VOUT=00		1.8		V
V_{FD2}	Field detect output voltage	EH_FD_VOUT=01		1.5		V
V_{FD3}	Field detect output voltage	EH_FD_VOUT=10		2.5		V
V_{FD4}	Field detect output voltage	EH_FD_VOUT=11		3.3		V
V_{EH1}	Energy harvesting output voltage	EH_FD_VOUT=00		1.8		V
V_{EH2}	Energy harvesting output voltage	EH_ FD_VOUT=01		1.5		V
V_{EH3}	Energy harvesting output voltage	EH_ FD_VOUT=10		2.5		V
V_{EH4}	Energy harvesting output voltage	EH_ FD_VOUT=11		3.3		V
I_{EH1}	Energy harvesting output current	EH_ILIM=00		no limit		mA
I_{EH2}	Energy harvesting output current	EH_ILIM=01		2		mA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{EH3}	Energy harvesting output current	EH_ILIM=10		1		mA
I_{EH4}	Energy harvesting output current	EH_ILIM=11		0.5		mA

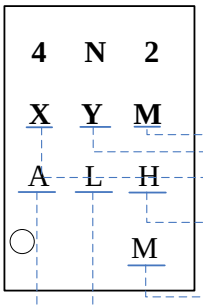
Note: 1. LCR meter, TA = 25°C, fi =13.56MHz, 2V RMS.

12 Ordering Information



13 Part Marking Scheme

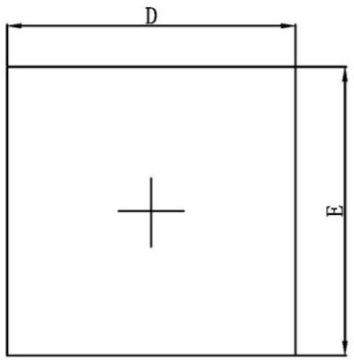
13.1 QFN16-3x3



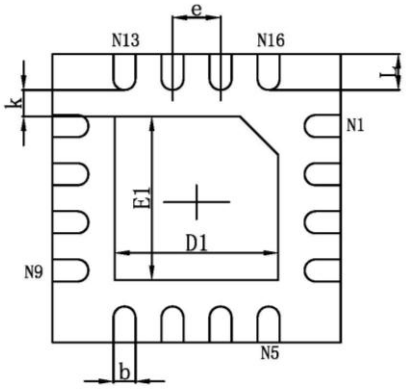
The month (hexadecimal digit) in which the products was molded.
The last one digit of the year In which the products was seal / molded.
Tag Density
HSF ID Code
G = RoHS Compliant, Halogen-free, Antimony-free
Moisture Sensitivity Level
1=MSL1
Lot Number（just with 0~9、A~Z）
Assembly’s Code

14 Packaging Information

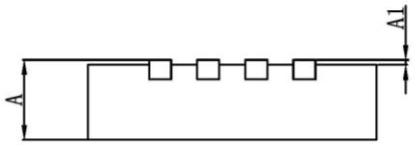
QFN16-3x3



Top View



Bottom View



Side View

Symbol	MIN	MAX
A	0.700/0.800	0.800/0.900
A1	0.000	0.050
D	2.924	3.076
E	2.924	3.076
D1	1.600	1.800
E1	1.600	1.800
k	0.200MIN.	
b	0.180	0.280
e	0.500TYP.	
L	0.324	0.476

NOTE:
1. **Dimensions are in Millimeters.**

15 Revision History

Version	Publication date	Pages	Revise Description
preliminary	Sep. 2016	137	Initial Document Release.

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